Modicon TSX Quantum

140 EHC 105 00
User Manual

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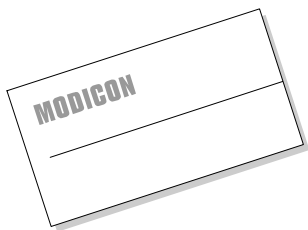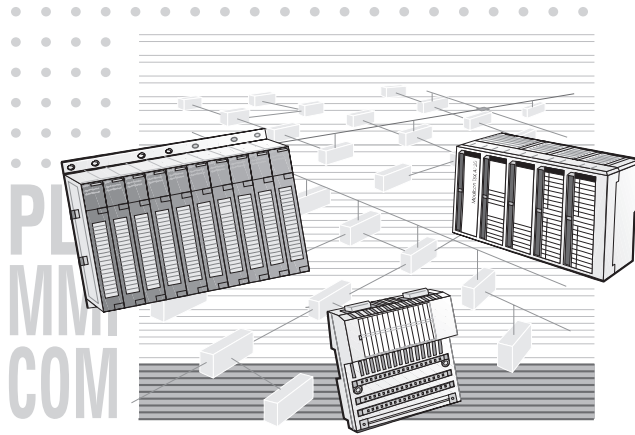
MODICON

GROUPE SCHNEIDER

■ Modicon ■ Square D ■ Telemecanique

140 EHC 105 00

High Speed Counter Module for

Modicon TSX Quantum

User Manual
Version 1.01

840 USE 443 00

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Contents

Symbols, Terminology, Abbreviations

Throughout this manual, the following visual aids highlight important and / or special information.

Note: Important, useful, or interesting information is shown as a note.

Caution: Cautions alert the reader of a possible hazard to the equipment or the product and then point out the propper procedure to avoid the hazard. Cautions also give the reader important instructions or strong suggestions to avert adverse consequences.

Warning: Warnings alert the reader of a possible hazard to personnel and then point out proper procedure to avoid the hazard.

Expert: This symbol is used when more detailed information is given, and is intended exclusively for experts (special training required). Skipping this information does not interfere with understanding the publication and does not restrict standard application of the product.

Tip: This symbol is used for Tips & Tricks.

Path: This symbol is a popup in the helptexts, this means you can click on it.

In software documentation this symbol tells you how to select the described menu commands and dialog boxes. The steps are always given starting from the main menu.

In EFB documentation (block libraries) this symbol tells you in which library and in which group you can find the described EFB.

Figures are given in the spelling corresponding to international practice and approved by SI (Système International d' Unités). I.e. a space between the thousands and a usage of a decimal point (e.g.: 12 345.67).

Declared Objectives

This User Manual, including the EHC 105 module description, is to serve as an aid to fast counter configuration.

Chapter 1 The operational characteristics of the EHC 105 are covered here.

Chapter 2 This chapter describes module configuration and parameterization.

Chapter 3 Four configuration examples are covered in this chapter.

Chapter 4 In this chapter the EHC 105 derived data types are presented.

Appendix A This chapter contains the module description.

Related Documents

Title	Örder Reference
Modicon TSX Quantum Automation Series, Hardware Reference Guide	840 USE 100 00 (Version 5.0)
Modbus Plus Network, User's Manual	890 USE 100 02
Modicon Modlink, User's Guide	GM–MLNK–001
Modicon IBM Host Based Devices, User's Guide	GM–HBDS–001
BM85 Modbus Plus Bridge / Multiplexer, User's Guide	GM–BM85–001

Validity References

The primary basis of this documentation is the EHC 105 module HW index level 12.02 and firmware version 2.0.7. The corresponding configuration software is Concept >= Release 2.0 or Modsoft >= Release 2.4.

☞ **Note:** The latest information can be found in the Concept README.WRI file.

Chapter 1
Introduction to the EHC 105

The following topics will be reviewed:

☐ Introduction

☐ Operational Characteristics

☐ EHC 105 Counter Types

☐ State RAM Structure

☐ Monitoring Capabilities

☐ Start–Up Characteristics

1.1 Introduction

1.1.1 General

The EHC 105 module is a high–speed counter module for the Modicon TSX Quantum controller.

Counting frequencies of up to 100 kHz can be monitored, depending upon cable length, transmitter type and voltage refer to Modul description page 98, Table 14.

The EHC 105 includes 5 independent counters, each counter can be operated with either 5 or 24 VDC pulse input signals. The counters can be operated in the following operating modes:

☐ Event counter, 32–bit, with four distinct operating modes

☐ Differential counter, 32–bit, with two distinct operating modes

☐ Repetitive counter, 16–bit

☐ Rate counter, 32–bit, with two distinct operating modes

There are eight isolated, discrete inputs and eight isolated, discrete outputs (24 VDC level) available. These discrete I/Os can be assigned to the various signals of the individual counters.

This module is software configurable with Concept or Modsoft.

Configuration Information is transfered from the controller to the EHC 105 module only at controller start up or module hot swap.

Data transfer of the set point and actual values is exchanged every scan cycle.

The user program is processed in the controller.

The EHC105 module functions asynchronously with the controller, allowing fast response and control.

☞ **Note:** Certain parameter defaults are assigned at module start–up, which among other things, assign specific functions to the discrete inputs (refer to page 34 Discrete I/O start–up assignments).

The EHC 105 is using with Modsoft or Concept.

1.1.2 Using Concept and Modsoft

The following menu selection of terms for Concept and Modsoft are presented below and are described in this chapter.

Menu Selection Terms:

Concept 2.0	**Modsoft 2.4**
Output Switch–Off	Output Switch–Off
Preceded Signal	Set Point
Preceded Set Point	Output Set Point
Final Signal	Final Set Point
Final Signal Value	Final Set Point Value
Dynamic Final Signal	Timed Final Set Point
Clock Watchdog Time	Counter Watchdog Time
Clock Enable	Counter Enable
Invert Clock	Input Signal counts on:
	–Pos. Transition
	–Neg. Transition

For configuration, Concept offers five dialog screens and Modsoft 10 dialog screens.

1.2   Operational Characteristics

Local Subrack   RIO Subrack   DIO Subrack

CPS | CPU | EHC 105 | CRP 931   CPS | CRA 931 | EHC 105   CRA 211 | EHC 105

RIO Bus

MB+

MB+   Concept or Modsoft
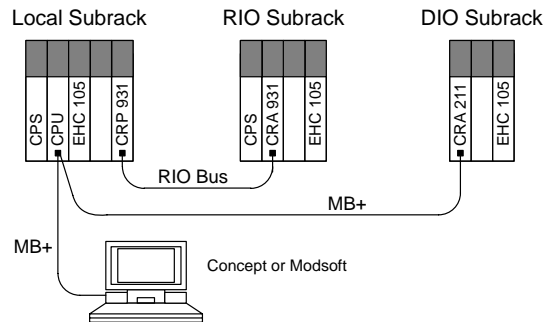
Figure 1   Typical hardware configuration

CPU

State RAM

4xxx
OUT
(13x)

3xxx
IN
(12x)

Parameters

EHC

Data
Exchange   EHC
Program
Parameters   (Firmware)
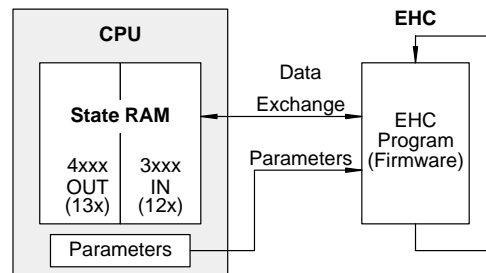
The counter module EHC105 needs 13
Out–register (4x...) and 12 In register (3x...) for
configuration.

Figure 2   State RAM diagram as used by the counter

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1.2.1 EHC 105 Counter Channel Principles
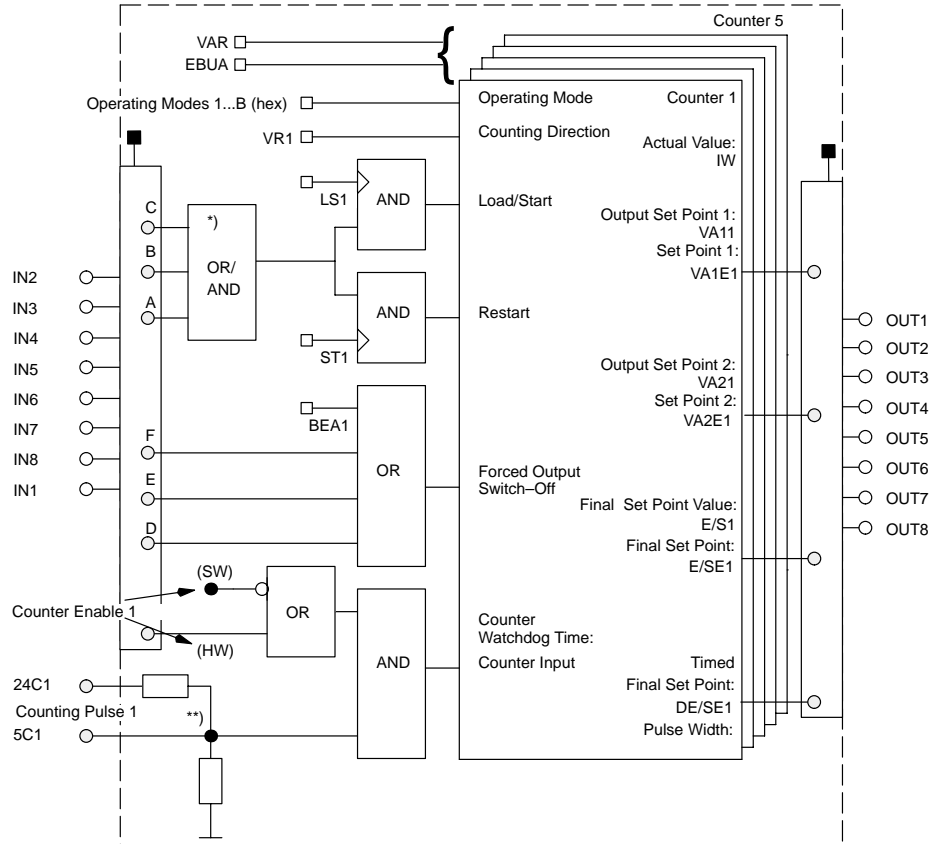
*) Configurable as either AND or OR. If the gate is not configured the output from this gate is TRUE.

**) The counting pulse input voltage divider has been schematically simplified

○— Discrete input signals   □— State RAM
—○ Discrete output signals   —○| Inversion
●— Parameters from the Concept/Modsoft configuration dialog
■ Discrete IN/OUT assignments to the internal counter signals and possible I/O inversions (through a configuration dialog).

Figure 3   Counter block diagram (counter 1 is depicted)

1.2.2 Description of the Individual Signals

IN1 ... 8: Discrete input signals which can be connected and individually inverted to the counter's control inputs .

☐ Each INx signal may be selected several times.
☐ Every input may be assigned the load/start, restart, or forced Output switch–off functions.
☐ Inputs can also be used as counter enable. However in this case the allocations are defined and **may not be changed** (i.e. IN1 is allocated counter 1, IN2 to counter 2, etc.).
☐ The response times (including firmware scans) are :
  ☐ 10 ms for inputs IN1...IN6,
  ☐ 5 ms for the IN7 and IN8 inputs.
☐ Each discrete input can be inverted through the configuration dialogs.

☞ **Note:** The default is "Not inverted". For default assignement refer to page 34, chapter1.6 Start up characteristics.

24Cx/5Cx (x = 1...5): Discrete inputs for 24/5 VDC counting pulses.

☐ If the "Input Signal counts on:" is not selected ("Invert clock" in Concept 2.0) the counter will count on the "Neg. Transition".
☐ If the selection is made, the counter will count on the "Pos. Transition".

☞ **Note:** The default is "Neg. Transition".

VAR: is a bit within an output register (4x...), which determines if the Output Set Points will be relative or absolute to Final Set Point Value for all 5 counters.

☐ "1" signal: Output Set Point is relative (to the Final Set Point Value)
☐ "0" signal: Output Set Point is absolute.

☞ **Note:** Before configuration, the value is 0.

EBUA: Is an output register (4x...) bit, which determines module switch–off behavior for all 5 counters when communication between the controller and EHC 105 is interrupted.

☐ "1" signal: The current output state is retained.
☐ "0" signal: All used outputs are set to "0" level.

Operating modes 1...B: One of 11 possible operating modes that can be selected for each counter through a 4x register (Refer to page 31 ore 16).

☞ **Note:** Before configuration mode is same as mode A. The remaining operating modes (0, C, D, E, F) are equal to the mode A.

VRx (x = 1...5): Is a bit within an output register (4x...), which determines the counting direction of the associated counter. (See also Counting Direction page 14)

☐ "1" signal: Down
☐ "0" signal: Up

☞ **Note:** Before configuration, the value is 0.

LSx (x = 1...5): Load/start counter is a bit within an output register (4x...), minimum pulse width: 3 ms. For more information refer to Figure 4 and Figure 5 on page 12 and 13 Relationship diagrams.

☞ **Note:** Before configuration, the value is 0.

BEAx (x = 1...5): Output Switch–Off is a bit within an output register (4x...). The pulse must be at least 3ms width.
When BEAx is "1", it latches the current count in a buffer. While the counter continues to count, VA1Ex, VA2Ex and E/SEx are reset. This is also true for any assigned outputs Outx. For more information refer to Figure 4 and Figure 5 on page 12 and 13 Relationship diagrams.

☞ **Note:** Before configuration, the value is 0.

STx (x = 1...5): Counter restart is a bit within an output register (4x...), minimum pulse width: 3 ms.
STx signal releases buffer and counter value of equal current value.
For more information refer to Figure 4 and Figure 5 on page 12 and 13 Relationship diagrams.

☞ **Note:** Before configuration, the value is 0.

Counter enable: These are two enable inputs which have the following functions:

☐ (SW) counter enable x (x = 1...5): software switch, that enables the counter and is activated from the Concept/Modsoft configuration screen. In Modsoft select the option as follow:
  ▫ "Use Input x for counter enable: Yes" : the (HW) counter enable is effective,
  ▫ "Use Input x for counter enable: No" : the counting pulse is always enabled.

☞ **Note:** The default is "Use Input x for counter enable: No" .

☐ (HW) counter enable x (x = 1...5): Is a signal that enables the counter, if "Use Input x for counter enable:" is Yes.
  Input channels for this function are predefined. IN1 is allocated to counter 1, IN2 is allocated to counter 2 etc.
  ▫ "1" signal: counter is enabled (Input not inverted).
  ▫ "0" signal: counter is disabled (Input not inverted).

☞ **Note:** The default: Input is not selectable for counter enable.

⚠ **Caution: The pulse counting begins after the first complete pulse following the counter enable signal. Accordingly, after counting pulse disable, the next counting pulse will still be registered. As a result during each count cycle (enable / disable), one pulse will be missing.**

Counter Watchdog Timer: This timer monitors incoming pulses and can be enabled throught the Concept / Modsoft dialog screen:

☐ Value 0: no monitoring
☐ Values 1...255: (x 0.1) sec

☞ **Note:** The default is value 0.

VA1x (x = 1...5): Is the first Output Set Point and can be configured through the Concept / Modsoft dialog screen.
Value range: 0...(2 exp31) −1

Note: The default is value 0.
If relative Output Set Point mode is selected, output Set Point Values are relative to the Final Set Point Value.
Requirement for that: E/S > VA1 >= VA2 >= 0.
If absolute Output Set Point mode is selected, this value is absolute.
Requirements for that: E/S > VA2 >= VA1 >= 0.

VA1Ex (x = 1...5): Is a bit within an input register (3x...).

☐ This may be assigned through the Concept / Modsoft dialog screen to any of the discrete outputs OUT1...OUT8.

Note: Before configuration, the value is 0. For default assignement refer to page 34, chapter1.6 Start up characteristics.

VA2x (x = 1...5): Is the second Output Set Point and can be configured through the the Concept / Modsoft dialog screens.
Value range: 0...(2 exp31) −1

Note: The default is value 0.
If relative Output Set Point mode is selected, output Set Point Values are relative to the Final Set Point Value.
Requirement for that: E/S > VA1 >= VA2 >= 0.
If absolute Output Set Point mode is selected, this value is absolute.
Requirements for that: E/S > VA2 >= VA1 >= 0.

VA2Ex (x = 1...5): Is a bit within an input register (3x...).

☐ This may be assigned through the Concept / Modsoft dialog screen to any of the discrete outputs OUT1...OUT8.

Note: The default assignement refer to page 34, chapter1.6 Start up characteristics.

E/Sx (x = 1...5): Is an output register (4x...) in which the counter's final (up counter) or inital (down counter) is entered.
Value range: 0...(2 exp31) −1

Note: Before configuration, the value is 0.

E/SEx (x = 1...5): Final Set Point is a bit within an input register (3x...).

□ This may be assigned through the Concept / Modsoft dialog screen to any of the discrete outputs OUT1...OUT8.

☞ **Note:** Before configuration, the value is 0. For default assignement refer to page 34, chapter1.6 Start up characteristics.

DE/SEx (x = 1...5): The Timed Final Set Point, settable through the Concept / Modsoft dialog screen:

□ This may be assigned through the Concept / Modsoft dialog screen to any of the discrete outputs OUT1...OUT8.

☞ **Note:** Before configuration, the value is 0. The default assignement is: No assignement.

Pulse width: This defines the length of the Timed Final Set Point pulse. In addition, in operating mode A, this defines the time for all associated outputs.

□ Value 0: output DE/SEx is disabled
□ Values 1...255: (x 0.02) sec.

☞ **Note:** The default value is 0.

🛑 **Warning: If in operating mode A, this value equal "0" there will be no outputs.**

OUT1...8: Discrete output signals, which can be assigned and individually inverted to the counter outputs VA1E (Set Point 1), VA2E (Set Point 2), E/SE (Final Set Point), and DE/SE (Timed Final Set Point).

☞ **Note:** The default: outputs are not inverted. The default assignment refer to page 34, chapter1.6 Start up characteristics.

🛑 **Warning: Do not select the same output OUT1 ... OUT8 with more than one Set Point. Even if Modsoft allowed you to do that, such multiple use is prohibited. Such double assignments lead to unpredictable process states, and are particularly difficult to diagnose.**

1.2.3 Output Set Point Mode (Absolute, Relative)

The Output Set Point is configured once for all module counters.

The module operates in absolute or relative Output Set Point Mode.

1.2.3.1 Absolute Output Set Point Mode
In this mode, the value entered in the Concept / Modsoft screen is the actual Output Set Point.

1.2.3.2 Relative Output Set Point Mode
In this mode, the Output Set Point is the difference between the entered value in the Concept / Modsoft screen and the Final Set Point Value.

1.2.4 Start and Stop Function Priority Rankings

The prioritazing of signals to start or stop a counter is as follow:

Priority 1   Forced Output Switch–Off, active for BEAx = "1" (state RAM) OR one of the configured discrete inputs as "1".

Priority 2   Load/start counter, active for LSx = "1" (state RAM) AND a TRUE evaluation of the configured discrete inputs.

Priority 3   Restart counter, active for STx = "1" (state RAM) AND a TRUE evaluation of the configured discrete inputs.

☞ **Note:**   The user program commands are necessary for starting and restarting of the counting procedures. Setting of the corresponding discrete inputs is also required. When no discrete input is assigned to the commands through "Load/Start and Restart", the counting procedure is initiated through the output status word (4x...) bits LSx resp. STx.

1.2.4.1 Relationship Diagrams of LS1, ST1, and BEA1 for Counter 1

Without hardware input configuration (Load/Start, Restart, Output–Switch–Off and Counter Enable).

DE/SE1 pulse width can be specified in the Concept/Modsoft configuration screen.
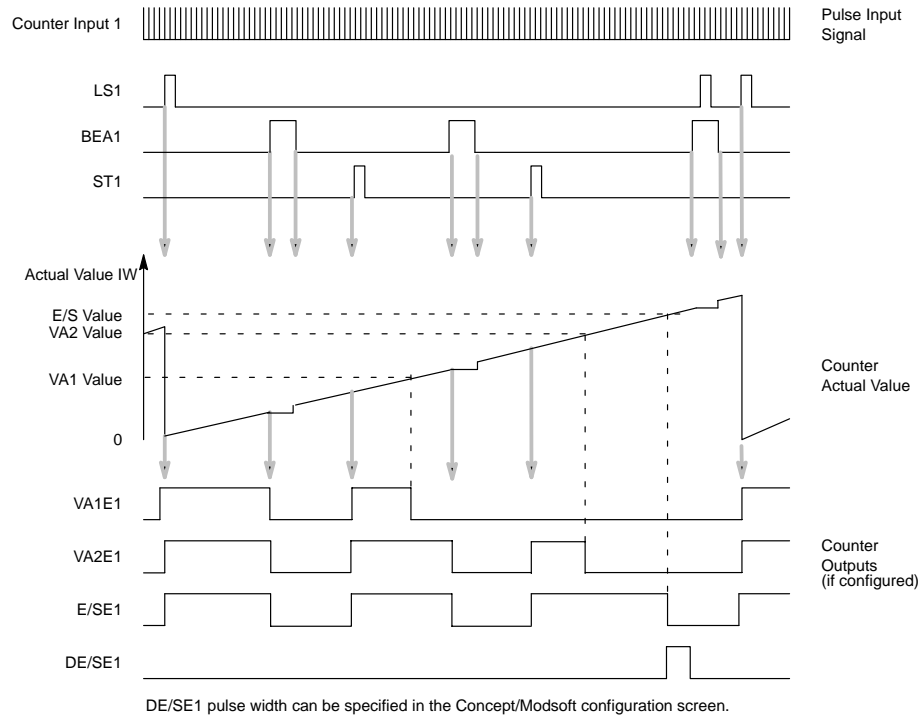
Figure 4   Counter 1 diagram as event counter, parallel, absolute, output function non inverted and counting up

LS1: With the rising edge from LS1, the actual counting value is set to 0. The outputs VA1E1, VA2E1 and E/SE1 are set to "1" signal for the operation mode 1 ... 5 and 8,9 or to "0" signal for operation mode A and B.

BEA1 / ST1: With a "1" signal at BEA1 the actual value will latch; the counting continues in an internal memory of the module. Is there on BEA1 a "0" signal the counting of the actual value continues with the current contents of the memory. Is there on ST1 a rising edge the outputs switche on depended from the actuale value.

With hardware input configuration (Load/Start, Restart, Output–Switch–Off and Counter Enable).
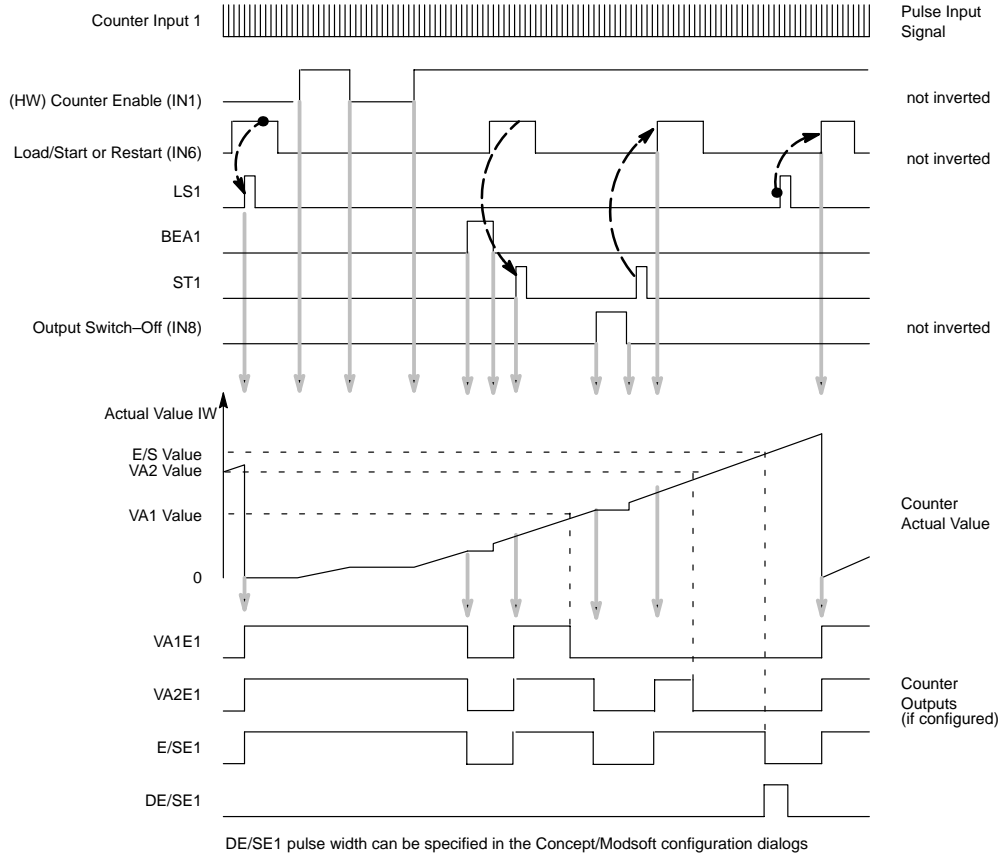
Figure 5   Counter 1 diagram as event counter, parallel, absolute, with output function non inverted and counting up

👉 **Note:** The discrete input evaluation for "Load/Start or Restart" is AND'ed with the LSx resp. STx signal. The LSx and STx signals operate edge–controlled.

👉 **Note:** The "Output Switch–Off" discrete inputs have the same function as the BEAx bit.

The AND condition is true should there have been no configuration carried out for "Load/Start or Restart"; the LSx and STx bits then function alone.

If the discrete input is not inverted, the High signal is active (see figure above). If discrete input is inverted, the Low signal is active. LSx and STx bit are always active with the rising ege, it can not be inverted.

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BEAx is always active with the High signal, it can not be inverted.
An active BEA signal set all inverted outputs to a High signal.
If the Outputs are inverted, the state from the signals VA1Ex, VA2Ex and E/SEx
will not inverted.

1.2.5   Counting Direction Determination

The individual counters can function as bidirectional counters, counting up or
down. The counting direction is specified by output status word (4x...) bit VR.

☐ VRx = "0": Up–counter, starting with 0, stop at final value E/S.
☐ VRx = "1": Down–counter, starting at initial value E/S, stop at 0

☞ **Note:**   Do not change the value of the VRx bit during operation of the counter.
If the value changes, the associated outputs of the counter will be switched off.

1.2.6 Overview and Relationships of Counter Functionality Features

Settings overview

Per Module

Per Counter

Down

BA=operating mode (hex)

Relative mode

Outputs Remain

VAR = 1
VAR = 0

EBUA = 1
EBUA = 0

VAR = 1
VAR = 0

Outputs Switch Off

Absolute mode

BA = A VR = 1 / 0 Event/Timed

BA = 1 VR = 1 / 0 Event/Parallel

BA = 8 VR = 1 / 0 Event/parallel/fast *)

BA = 2 VR = 1 / 0 Event/Serial

BA = 9 VR = 1 / 0 Event/Serial/Fast *)

BA = B VR = 1 / 0 Event/Latched

BA = 3 VR = 1 / 0 Differential/Parallel

BA = 4 VR = 1 / 0 Differential/Serial

BA = 5 VR = 1 / 0 Repetitive

Up

EBUA and VAR selection have no effect to this type of counter in operating modes 6 and 7.

BA = 6 VR = 1 / 0 Rate Counter 100ms

BA = 7 VR = 1 / 0 Rate Counter 1sec

*) Fast counters have no restart function

Figure 6 Possible counter settings

1.3   EHC 105 Counter Types

The EHC 105 module can operate as:

☐ Event counter (with and without fast Final Set Point)
☐ Event counter with Timed or latched outputs
☐ Differential counter (without fast Final Set Point)
☐ Repetitive counter (with fast Final Set Point)
☐ Rate counter

The selection of the various counter types takes place through the operating mode selections in state RAM. Every counter type can count up and down. Output Set Point Mode can be set to be relative (to the Final Set Point Value) or absolute.

☞ **Note:**   For an active counter, any change of the operating mode or counting direction, switch–off behavior, or type of Set Point triggers an Output Switch–Off. A change of the operating mode accompanied by load/start is not possible. (The setting of the load / start bit after changing the operation mode must be done in the next scan cycle.)

☞ **Note:**   Discrete Output Signal Response Times:
Without fast Final Set Point: typically 3 ms.
With fast Final Set Point: typically 0.5 ms.

Table 1   Counter Operating modes

Value (hex)	Meaning
1	Event counter with parallel Set Point activations
2	Event counter with serial Set Point activations
3	Differential counter with parallel Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive)
4	Differential counter with serial Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive)
5	Repetitive counter
6	Rate counter, gate time t = 100 ms
7	Rate counter, gate time t = 1 s
8	Event counter with parallel Set Point activations and fast Final Set Point
9	Event counter with serial Set Point activations and fast Final Set Point
A (default)	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs.

Table 1   Counter Operating modes

Value (hex)	Meaning
B	Event counter with latched Set Point outputs.
0, C, D, E, F	as operating mode A

1.3.1   The Event Counter

The event counter is a gate–controlled, bidirectional counter with two or less Set Points, a Final Set Point and a Timed Final Set Point. It utilizes six different operating modes. See also Table 5 on page 31.

☐ Operating mode A: with adjustable "time on" outputs
    ☐ The pulse width configuration applies the same value to all counter outputs. Outputs are at "0" signal on start.
☐ Operating mode 1: with parallel Output Set Point activation
☐ Operating mode 2: with serial Output Set Point activation
☐ Operating mode 8: with parallel Output Set Point activation and fast Final Set Point
☐ Operating mode 9: with serial Output Set Point activation and fast Final Set Point
☐ Operating mode B: with latched Set Point activation
Outputs are at "0" signal on start.

The value range for all operating modes amounts to: $0...(2 \exp 31) - 1$, except the operating mode 5 is $0...(2 \exp 16) - 1$.

1.3.1.1 Operating modes 1 and 8 (Event counter with relative Output Set Point Value and parallel Set Point activation)
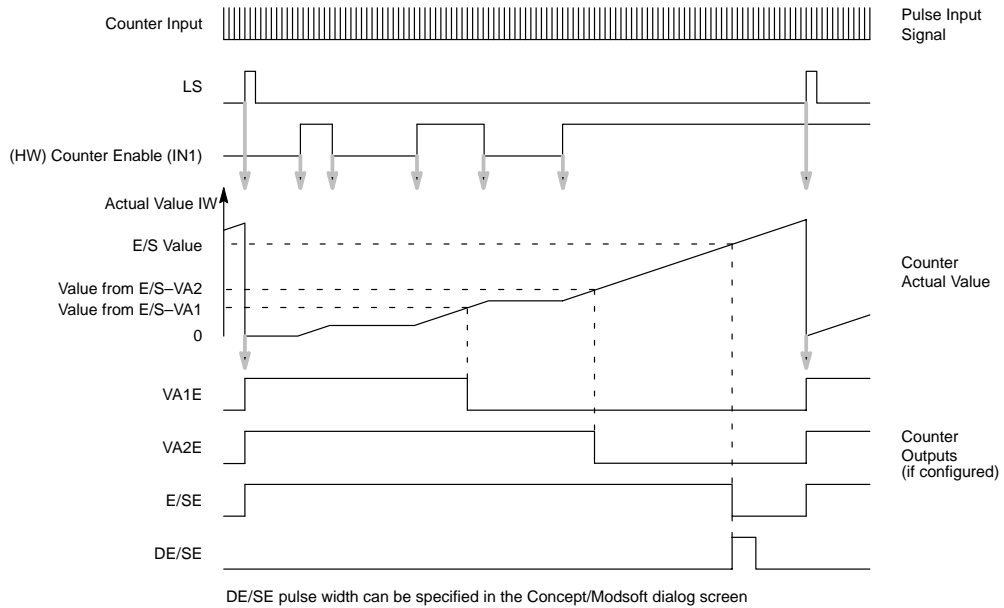
Figure 7   Counting up (VR = 0)
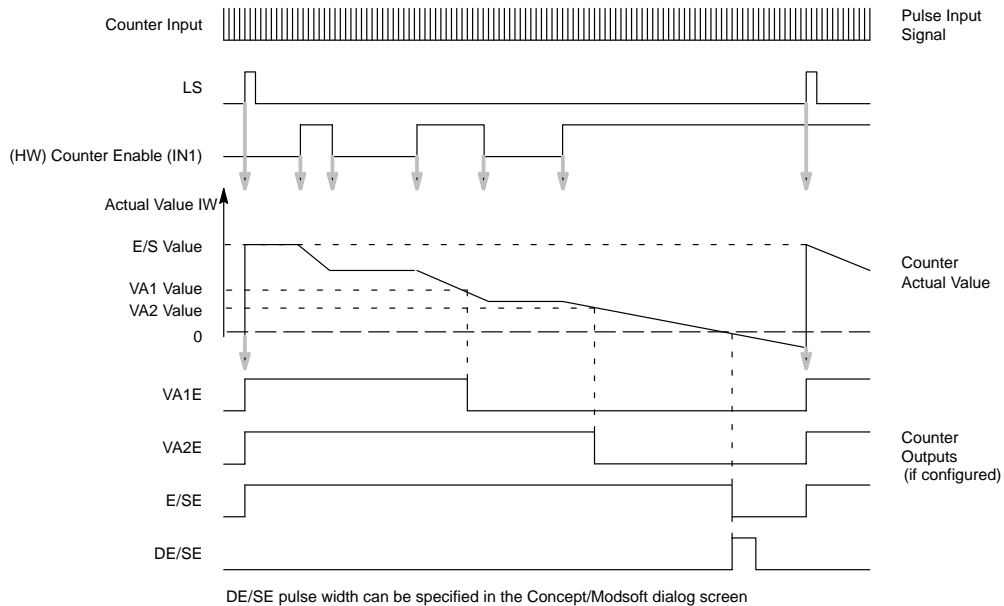
Figure 8   Counting down (VR = 1)

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1.3.1.2 Operating modes 2 and 9 (Event counter with relative Output Set Point Value and serial Set Point activation)
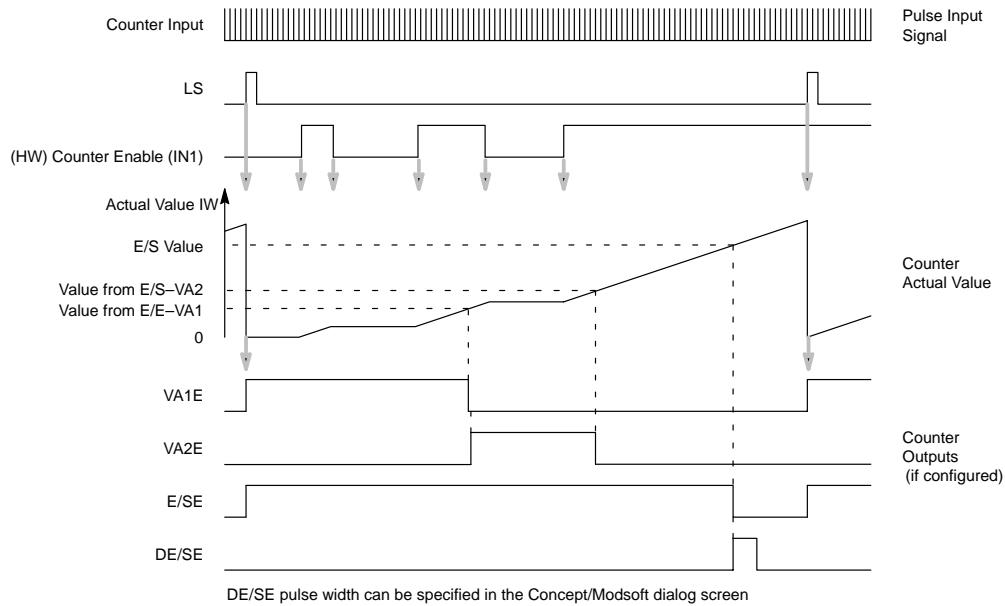
Figure 9 Counting up (VR = 0)

Figure 7 to Figure 9 Event counter with relative and parallel and serial Set Point activation are typical time diagrams.
That do no take into account the following signals:

☐ BEAx Further information you will find on page 12

☐ STx Further information you will find on page 12

☞ **Note:** STx has no function in the operating modes 8 and 9.

1.3.1.3 Operation mode A (Event counter with absolute Output Set Point Value and timed output activation)

A **common** pulse width for **all** outputs can be specified in the Concept/Modsoft dialog screens
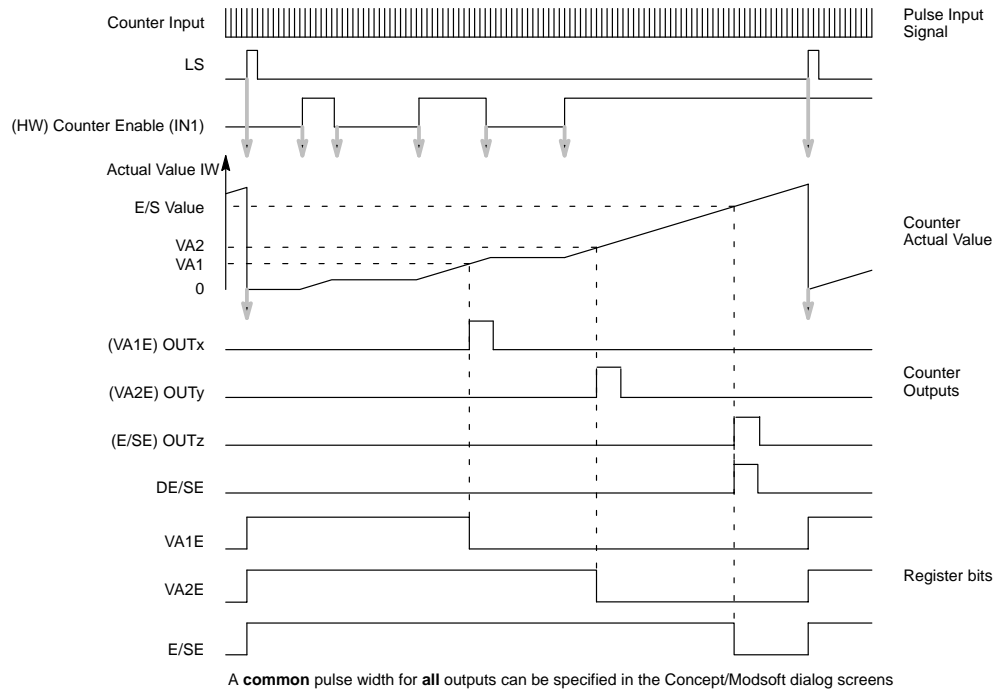
Figure 10   Counting up (VR = "0")

☞ **Note:** The activation of the discrete outputs are different from the activation of the register bits.

1.3.1.4 Operation–mode B (Event counter with absolute Output Set Point Value and latched output activation)

DE/SE pulse width can be specified in the Concept/Modsoft dialog screen
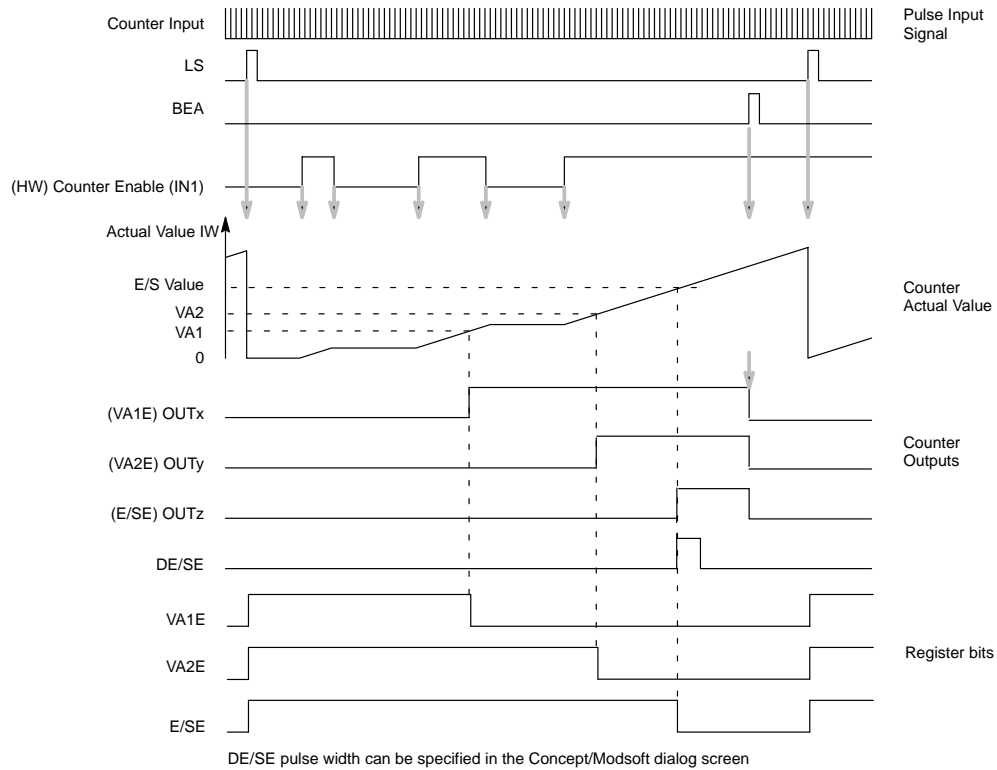
Figure 11   Counting up (VR = 0)

☞ **Note:**   The activation of the discrete outputs are different from the activation of the register bits.

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1.3.2 The Differential Counter

The differential counter is a gate–controlled counter with up to two Output Set Points, a Final Set Point and a Timed Final Set Point. A differential counter consists of two counter channels and meassures the difference of each of their pulses. It is equipped with two different operating modes:

☐ Operating mode 3: with parallel Set Point activation

☐ Operating mode 4: with serial Set Point activation

Counter 1 (clockwise) and 2 (counterclockwise) form a differential counter 1, while counter 3 (clockwise) and 4 (counterclockwise) form a differential counter 2. This configuration cannot be changed.

The counting value is determined from the difference of the two counters.

Differential counter configuration, control and evaluation is done through the parameters and values of the first counter with the exception of the counter input.

The configuration for the respective second counter must be performed separately. The parameter choices (from the Modsoft / Concept dialog screen) are:

☐ Invert Counter Input / Input Signal counts on.

☐ Use Input for Counter enable / Input for Counter enable.

☞ **Note:** A fast Final Set Point cannot be set for differential counters. If a counter is disabled, counter time monitoring is suspended.

☐ The value ranges are as follows:

  ☐ Set Point values: $0...(2\ \text{exp}\ 30)\ -1$
  ☐ Actual values: $-(2\ \text{exp}\ 30)...(2\ \text{exp}\ 30)\ -1$

☞ **Note:** The value range allows the differential counter to also be used for continuous monitoring.

1.3.2.1 Operating mode 3 (Differential counter with relative Output Set Point Value and parallel output activation)
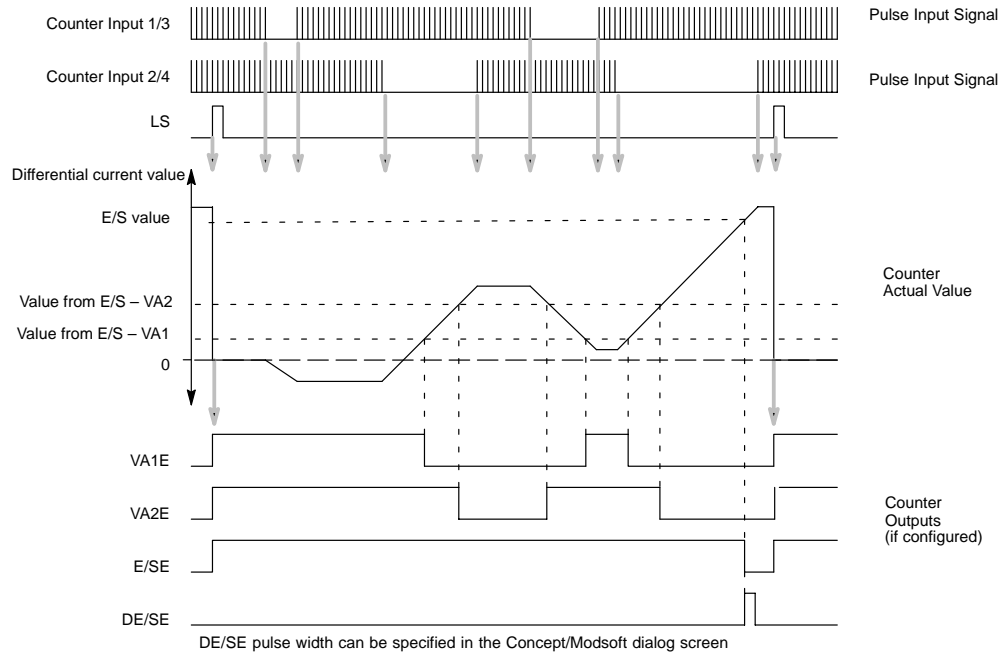
Figure 12 Differential counter with parallel output activation counts up (VR = 0)

Continuation Operating Mode 3 (Differential counter with relative Output Set Point Value and parallel output activation)

Figure 13   Differntial counter with parallel output activation counts down (VR = 1)
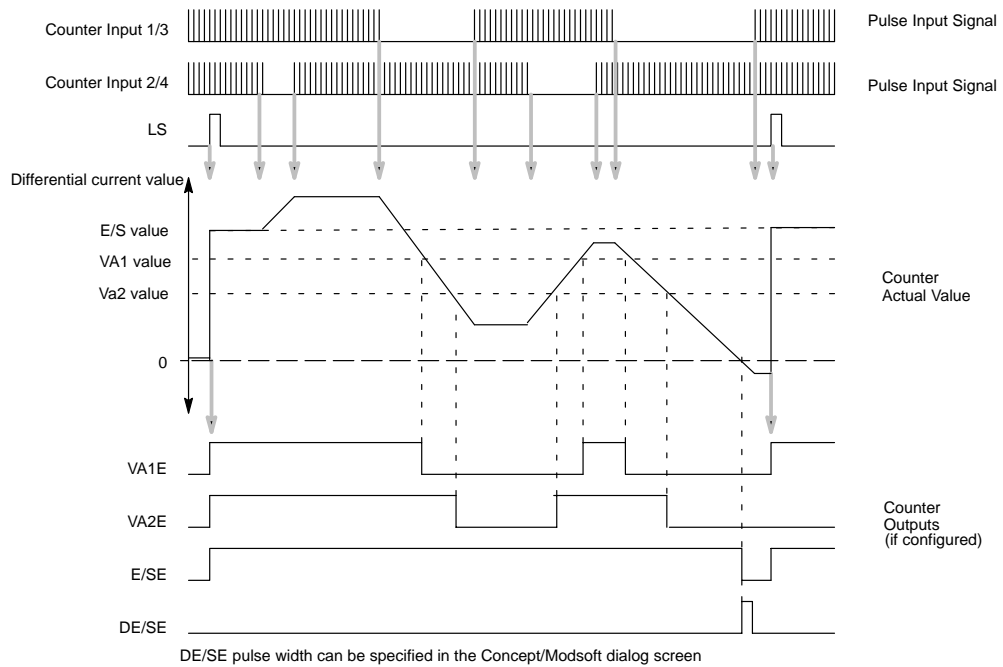
Figure 12 and Figure 13 "Differential counter with parallel set–point cutoffs (VR = 0)" are typical timing diagram that do not take into account the following signals:

☐ BEAx Further information you will find on page 12

☐ STx Further information you will find on page 12

1.3.2.2 Operating mode 4 (Differential counter with relative Output Set Point Value and serial output activation)
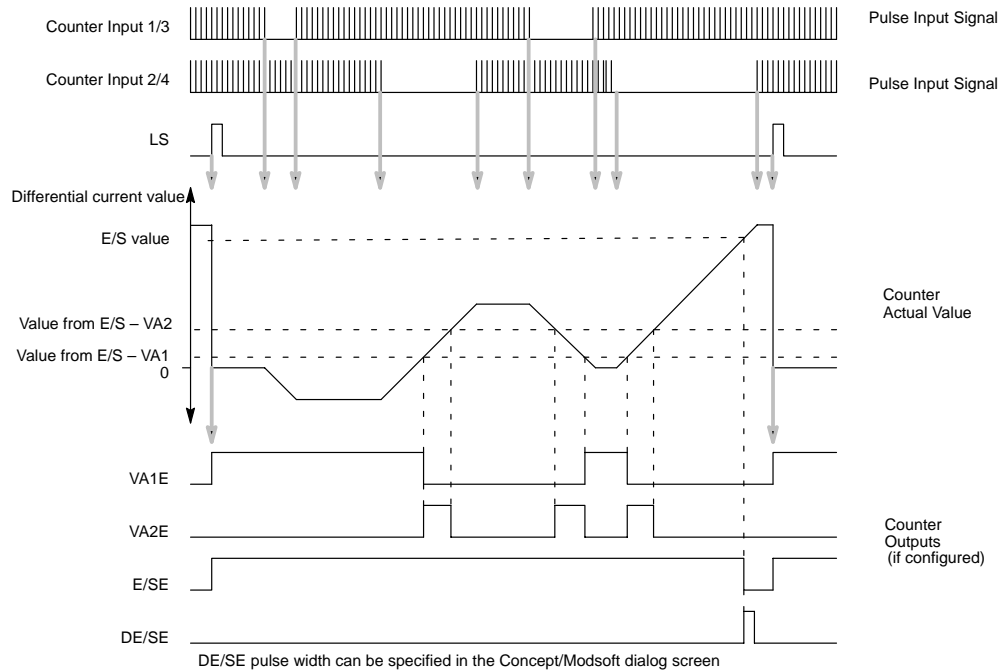
Figure 14 Differential counter with serial output activation counts up (VR = 0)

Figure 14 "Differential counter with serial set–point cutoffs" is a typical timing diagram that do not take into the following signals:

☐ BEAxFurther information you will find on page 12

☐ STxFurther information you will find on page 12

1.3.3 The Repetitive Counter (Operating mode 5)

The repetitive counter is an up / down counter with up to two Output Set Points, a fast Final Set Point, which acts as a third Set Point and a Timed Final Set Point.

☐ Operating Mode 5: with serial output activation

As a repetitive counter, every time the Final Set Point value is reached, the following restrictions apply:

☐ E/Sx values are limited to the value ranges 0...(2 exp 16) −1.
☐ The Final Set Point value cannot be changed when the counter is active. BEA must be set in advance.
☐ The Final Set Point Value must be equal or greater than 2.

DE/SE pulse width can be specified in the Concept/Modsoft dialog screen
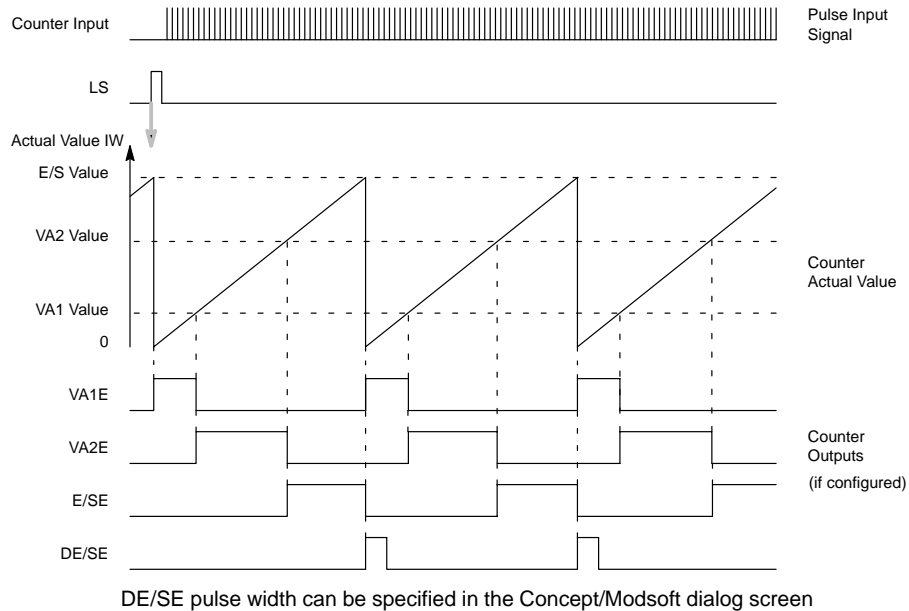
Figure 15   Repetitive counter with serial output activation

Figure 15 "Repetitive counter" is a typical timing diagram that does not take into account the following signal:

☐ BEAxFurther information you will find on page 12

☐ STx has no effect in this operating mode refer to page 12 for further information

1.3.4 The Rate Counter (Operating mode 6 or 7)

The rate counter counts the number of pulses per unit time. A unit time is specified with the choice of the operating modes 6 or 7. The read value is then saved as the actual value.

The determined actual value thus represents the pulse count per unit time, and can be used to determine velocities, flow rates, or even revolutions.

Inputs and outputs are not processed in this counter type.

THe Watchdog timer function is not supported.

There are two operating modes for the rate counter. These differ only in the prescribed internal gate time.

☐ Operating mode 6: The gate time t amounts to 100 ms

☐ Operating mode 7: The gate time t amounts to 1 s

1.4 State RAM Structure

1.4.1 Input Structure

Table 2   State RAM input structure (EHC 105 –> CPU), word addressing

3x Registers	Relative Ad- dress		Content
3x	000		Input Status Word 1
3x+1	001		Input Status Word 2
3x+2	002	Low Word	Counter 1
3x+3		High Word	Actual Value
3x+4	004	Low Word	Counter 2
3x+5		High Word	Actual Value
3x+6	006	Low Word	Counter 3
3x+7		High Word	Actual Value
3x+8	008	Low Word	Counter 4
3x+9		High Word	Actual Value
3x+10	010	Low Word	Counter 5
3x+11		High Word	Actual Value

Quantum local drop:
The relative address relates to the Concept configuration "In Ref" address,
 refer to Configuration Steps in chapter 2.2.2.1, page 39.

Modsoft Configuration:
The relative address relates to the Modsoft configuration "Input Ref" address,
 refer to Configuration Steps, chapter 2.2.3.1, page 42.

☞ **Note:**   Counter actual values are shown as decimal values: in Concept as Dec
(signed 32–bit); in Modsoft as Long Dec (unsigned 32–bit) for CPU Exec 2.0
and greather. This means that negative values can not be displayed correctly.

Input Status Word 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3x				E/SE5	E/SE4	E/SE3	E/SE2	E/SE1	US24	SC	INDI–CATE	ERR5	ERR4	ERR3	ERR2	ERR1

MSB   LSB

Input Status Word 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
3x+1				VA2E5	VA2E4	VA2E3	VA2E2	VA2E1				VA1E5	VA1E4	VA1E3	VA1E2	VA1E1

MSB   LSB

MSB = most significant bit
LSB = least significant bit

Table 3   Input status word signal explanations

Signal	Va-lue	Meaning
Input Status Word 1		
ERRx	1	Error in counter x (specified by Indicate, i.e. bit 5 in status word 1)
INDICATE	0	Counter overflow (actual value > 2 exp (16), 2 exp (30) resp. 2 exp (31)–1)
	1	Counting pulse error (counter timeout value expired)
SC	1	Discrete output short circuit or overload
US24	1	External power failure (discrete outputs)
E/SEx	1	Final set point signal on counter x is 1 Signal
Input Status Word 2		
VA1Ex	1	First Set Point signal on counter x is a 1 Signal
VA2Ex	1	Second Set Point signal on counter x is a 1 Signal

☞ **Note:** Output inversions (E/SEx, VA1Ex, VA2Ex) are not used on the corresponding bits in status words 1 and 2.

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1.4.2 Output Structure

Table 4 State RAM output structure (CPU –> EHC 105), word addressing

4x Register	Relative Address		Content	
4x	000		Output Control Word 1	
4x+1	001		Output Control Word 2	
4x+2	002		Output Control Word 3	
			Counter 1	
4x+3	003	Low Word	Stop value	for VR1 = "0", Final Set Point Value E/S1
4x+4		High Word	Initial value	for VR1 = "1", Final Set Point Value E/S1
			Counter 2	
4x+5	005	Low Word	Stop value	for VR2 = "0", Final Set Point Value E/S2
4x+6		High Word	Initial value	for VR2 = "1", Final Set Point Value E/S2
			Counter 3	
4x+7	007	Low Word	Stop value	for VR3 = "0", Final Set Point Value E/S3
4x+8		High Word	Initial value	for VR3 = "1", Final Set Point Value E/S3
			Counter 4	
4x+9	009	Low Word	Stop value	for VR4 = "0", Final Set Point Value E/S4
4x+10		High Word	Initial value	for VR4 = "1", Final Set Point Value E/S4
			Counter 5	
4x+11	011	Low Word	Stop value	for VR5 = "0", Final Set Point Value E/S5
4x+12		High Word	Initial value	for VR5 = "1", Final Set Point Value E/S5

Quantum local drop: The relative address relates to the Concept configuration "Out Ref" address, refer to (Configuration Steps chapter 2.2.2.1, page 39).

Modsoft Configuration: The relative address relates to the Modsoft configuration "Output Ref" address, (refer to Configuration Steps, chapter 2.2.3.1, page 42).

Output Control Word 1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4x	Counter 1 Operating Mode				VR1	BEA1	ST1	LS1			EBUA	VAR			FQ	Q

MSB   LSB

Output Control Word 2

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4x+1	Counter 3 Operating Mode				VR3	BEA3	ST3	LS3	Counter 2 Operating Mode				VR2	BEA2	ST2	LS2

MSB   LSB

Output Control Word 3

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4x+2	Counter 5 Operating Mode				VR5	BEA5	ST5	LS5	Counter 4 Operating Mode				VR4	BEA4	ST4	LS4

MSB   LSB
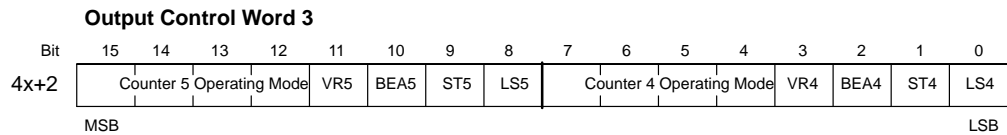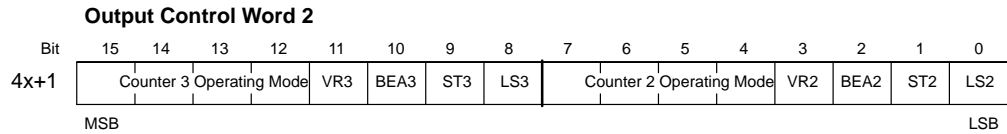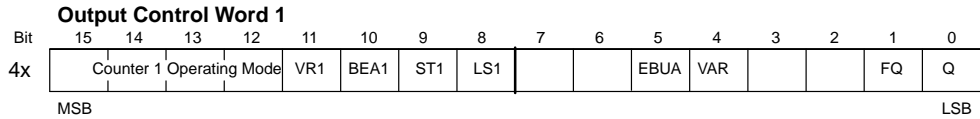
MSB = most significant bit
LSB = least significant bit

Table 5   Output control word signal explanations

Signal	Value (hex)	Meaning
Counter x Operating Mode	1	Event counter with parallel Set Point activations
	2	Event counter with serial Set Point activations
	3	Differential counter with parallel Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive)
	4	Differential counter with serial Set Point activations (only applies to counters 1 and 3, the Set Point and actual values of counters 2 resp. 4 are inactive)
	5	Repetitive counter
	6	Rate counter, gate time t = 100 ms
	7	Rate counter, gate time t = 1 s
	8	Event counter with parallel Set Point activations and fast Final Set Point
	9	Event counter with serial Set Point activations and fast Final Set Point
	A (default)	Event counter with timed "on" outputs, the pulse width setting holds for all employed outputs.
	B	Event counter with latched Set Point outputs.
	0, C, D, E, F	as operating modes A
VRx	0	Counter x counts up
	1	Counter x counts down
BEAx	1	Counter x Output Switch–Off
STx	1	Counter x restart (controlled by rising edge)
LSx	1	Counter x load/start (controlled by rising edge)
EBUA	1	Outputs retain their current state on communication errors
	0	Outputs go to "0" signal on communication errors

Table 5   Output control word signal explanations

Signal	Value (hex)	Meaning
VAR	1	Output Set Points (values) are relative for all counters
	0	Output Set Points (values) are absolute for all counters
Q	1	Acknowledgement for all counter channels after an output short circuit fault signal (SC). (The red LED (F) extinguishes).
FQ	1	Acknowledgement after power failure and counter errors (ERR1...ERR5 and Indicate). (The red LED (F) extinguishes). If several errors are present, they must be acknowledged individually one after the other.

Caution: If the counter's operating mode, counting direction, switch–off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

1.5   Monitoring Capabilities

1.5.1   Input Signal Monitoring

The EHC 105 can monitor the presence or absence of incoming signals. To activate signal monitoring, it is necessary to state a value between 1 and 255 in the Concept / Modsoft dialog screen for "Clock/Counter Watchdog Time". This fixes the counter's watchdog timers within the limits from 100 ms to 25.5 s. No monitoring is performed for 0 values.

If a pulse is not detected at the respective input of a running counter within the declared timeout interval, then the transmitter error flag (INDICATE) is changed to "1" and the corresponding error bit (ERR) is on, triggering a Forced Output Switch–Off and "F" LED is ON.

Counting pulse monitoring for the respective counter occurs when the counting pulse is enabled and the counter is running. The prerequisite is the specification of a watchdog timer: (Refer to page 6ff)

☞ **Note:**   Count pulse monitoring is not supported in operating modes 6 and 7. Refer to chapter 1.3.2, page 22 differential counters.

1.5.2   Quantum System Bus Monitoring

A "system active" signal is activated on the Quantum system bus. If the CPU fails, all outputs are set accordingly and the green ACTIVE status LED turns off.

The status of the outputs in the event of a communication failure between the controller and the EHC 105 can be selected through the EBUA output register bit (4x...).

☐ "1" signal: The current output state is retained.
☐ "0" signal: All employed outputs are set to "0" level.

1.5.3   US24 Power Monitoring

If the external 24VDC power supply fails during operation, the green "P" LED turns off and is shown in the module status byte and the red "F" LED turns on. If the power goes on again, the "P" LED turns on and the "F" LED turns off. An Output Switch–Off is not triggered for a running counter. The discrete output (OUT1...OUT8) status displays (1▶ to 8▶) turn off (independent from the defined output logic).

1.6 EHC 105 Start–Up Characteristics

At EHC 105 start–up, all actual values are cleared to 0, outputs are deactivated (i.e. VA1E=VA2E=E/SE =”0”) and the counters are defaulted to up–event counters, with absolute Output Set Point Values (VAR = ”0”) and outputs in timed control mode (operating mode A).
Outputs are set to ”0” (EBUA = ”0”) on controller communications failure with the EHC105.
By default, all counters are enabled.

Table 6 Start–up assignments for discrete I/O

Counter Input/Output	Discrete Signal	Pin Assignments
Counter 1		
LS1 (Load and Start)	IN1	21
ST1 (Restart)	IN1	21
BEA1 (Output Switch–Off)	IN6	26
Counting Pulse 1	5C1/24C1	1/11
VA2E1	OUT6	36
E/SE1	OUT1	31
Counter 2		
LS2 (Load and Start)	IN2	22
ST2 (Restart)	IN2	22
Counting Pulse 2	5C2/24C2	3/13
E/SE2	OUT2	32
Counter 3		
LS3 (Load and Start)	IN3	23
ST3 (Restart)	IN3	23
BEA3	IN7	27
Counting Pulse 3	5C3/24C3	5/15
VA2E3	OUT7	37
E/SE3	OUT3	33
Counter 4		
LS4 (Load and Start)	IN4	24
ST4 (Restart)	IN4	24
Counting Pulse 4	5C4/24C4	7/17
E/SE4	OUT4	34

Table 6   Start–up assignments for discrete I/O

Counter Input/Output	Discrete Signal	Pin Assignments
Counter 5		
LS5 (Load and Start)	IN5	25
ST5 (Restart)	IN5	25
Counting Pulse 5	5C5/24C5	9/19
BEA5	IN8	28
VA2E5	OUT8	38
E/SE5	OUT5	35

Chapter 2
Configuration

☐ Hardware and Software Prerequisites

☐ Configuration Steps

Configuration   37

2.1   Hardware and Software Prerequisites

☐ PC for Concept / Modsoft

☐ Software package: Concept $\geq$ version 2.0 or Modsoft $\geq$ version 2.4

☐ CPU EXEC $\geq$ version 2.0

☐ Quantum System with any CPU refer to "Quantum Reference Guide (840 USE 100 00)"

☞ **Note:**   Althought, this module is also supported with Modsoft 2.32, version 2.4 or greater is required. The screens, described in this document come from version 2.4.
This module is also supported with Concept 1.13, but we recommand to use version 2.0 or greater. The screens, described in this document come from version 2.0.

2.2   Configuration Steps

The steps necessary for configuration are presented here. Where additional information is necessary, references to the corresponding documentation is made.

2.2.1   Configuration Steps for Installation

☐ Configure your controller in accordance with your requirements, also with respect to the EHC 105, as described in the "Quantum Hardware Reference Guide (840 USE 100 00)". Details for connecting signal transmitters to the EHC 105 can be found within the module description in the appendix A (Module Description).

☐ Plan and carry out the module cabling in accordance with the module details (i.e. cable routing, shielding etc.).

☐ Log your terminal assignment plan on the label inlay inside the module I/O block cover.

2.2.2　Configuration using Concept ($\geq$ 2.0)

2.2.2.1　Drop configuration (slot and I/O map)

Local Quantum Drop							

Drop
Modules: 5　　　　Bits In: 224Bits Out: 240　　　Module Bits In: 192　Bits Out: 208
Status Table:　　　　　　　　　　　ASCII Port none ↓　　Delete　　Params...

Clear　　Prev　　Next　　　　　Cute　　Copy　　Paste

Slot	Module	Detected	In Ref	In End	Out Ref	Out End	Des ↑ p
1	CPS 214 00						DC PS 24V
2	CPU x13 0x						CPU 1xMB
3	DDI 353 00		100001	100032			DC IN 24V
4	DDO 353 00				000001	000032	DC OUT 2
5	...						
6	...						
7	...						
8	EHC 105 00		300001	300012	400001	400013	HIGH SPEI
9	...						
10	...						
11	...						
12	...						
13							↓

OK　　Cancel　　Help　　☐ Poll

Figure 16　Configuration using Concept

Table 7　Drop editor terminology explanations (see above)

Term	Meaning
Clear (Drop)	Configuration deletion for all slot resident modules
Delete (Module)	Deletion of the selected module
Params...	Starts the configuration dialog　　　　(see next screen)
Slot	Selects the slot for module entry
Module	Starts the module configuration dialog
Detected	Modules recognized on–line
In Ref	State RAM initial address (for input)
In End	State RAM calculated end address (for input)
Out Ref	State RAM initial address (for output)
Out End	State RAM calculated end address (for output)
Description	Short module description
OK	Accepts all inputs

2.2.2.2 Configuration of counter characteristics under Concept
The following EHC 105 settings are selected with the Concept dialog screen:

140 EHC 105 00

Inversion of Inputs
☐ No. 1   ☐ No. 2   ☐ No. 3   ☐ No. 4   ☐ No. 5   ☐ No. 6   ☐ No. 7   ☐ No. 8

Counter

Counter: 1 ▼

☐ Invert Clock   ☒ Input No. 1 for Clock Enable
Clock Watchdog Time (x 0.1s): 0

Preceded Setpoint
Value 1: 11   Value 2: 5

Inputs
Load/Start or Restart
Logic Between Start Inputs OR ▼
Input No: 6 ▼   Input No: – ▼   Input No: – ▼
Outputs Switch–Off
Input No: 8 ▼   Input No: – ▼   Input No: – ▼

Outputs
Preceded Signal 1
Output No: 1 ▼   ☐ Invert
Preceded Signal 2
Output No: 2 ▼   ☐ Invert
Final Signal
Output No: 3 ▼   ☐ Invert
Dynamic Final Signal
Output No: 4 ▼   ☐ Invert
Pulse Width (x 0.02 s): 20

OK	Cancel	Help

Figure 17   Concept dialog screen (counter 1 example)

Table 8   Quantum I/O map terminology explanations

Term	Meaning
Inversion of Inputs	Select inversion of all discrete inputs (IN1...IN8)
Counter	Selection of the individual counters
Invert Clock	Select inversion of the counter inputs
Input No. 1 for Clock Enable	Select Input 1 to enable counter.
Clock Watchdog Time (x 0.1s):	Counter Watchdog time setting in 0.1s steps, 0 disables counting pulse monitoring
Preceded Setpoint –Relative	If relative Output Set Point mode is selected, output Set Point Values are relative to the Final Set Point Value. Requirement for that: $E/S > VA1 >= VA2 >= 0$.
–Absolute	If absolute Output Set Point mode is selected, this value is absolute. Requirements for that: $E/S > VA2 >= VA1 >= 0$.
Logic Between Start Inputs	Logic function among inputs to Load / Start or Restart the counter.
Input No:	Assignment of up to 3 process inputs for load/start and restart function control.
Outputs Switch Off	Assignment of up to 3 process inputs to Output Switch–Off
Preceded Signal 1	Assignment (and optional inversion) of a discrete output to the first set–point.

Table 8 Quantum I/O map terminology explanations

Term	Meaning
Preceded Signal 2	Assignment (and optional inversion) of a discrete output to the second set–point.
Final Signal	Assignment (and optional inversion) of a discrete output to the final set–point.
Dynamic Final Signal	Assignment (and optional inversion) of a discrete output to the timed final set–point
Pulse Width (x 0.02s):	Setting of the Dynamic Final Signal pulse width (0...255). 0 disables the output.

2.2.3 Configuration under Modsoft ($\geq$ 2.4)

2.2.3.1 I / O Map screen

```
Utility         ClrDrop  HoldTime  ASCPort Drop      QUANTUM            Quit
F1 ──── F2 ──── F3 ──── F4 ──── F5 ──── F6 ──── F7─Lev 8─F8─OFF ── F9 ────
                              QUANTUM I/O MAP
    Type:  Local I/O         Head─Slot: 0        Drop:  1       Available:  444
    Drop Hold Up Time :  3  x100ms      Module Status Reg:  0
    Number of Inputs :   192            Number of Outputs :   208

    Slot        Module       Input Ref        Output Ref        Description
    101
    102
    103
    104
    105
    106
    107
    108    EHC 105 00     300100─300111  400100─400112  High Speed CTR 5CH
    109
    110
    111
    112
    113
    114
    115
    116
```

Figure 18   Configuration under Modsoft

Table 9   Quantum I/O map terminology explanations (see above)

Term	Meaning
F3 ClrDrop	Configuration deletion for all slot resident modules
Slot	Displays the slot for module entry
Module	Starts the module configuration dialog
Input Ref	State RAM initial address (for input)
Output Ref	State RAM initial address (for output)
Description	Short module description

2.2.3.2 Configuration of counter characteristics under Modsoft

The following EHC 105 settings are selected with the Modsoft configuration dialog, (the configuration dialog consists of 10 screen pages, an input and an output page per counter):

For Inputs

```
  Hex       Dec      Bin       GoTo                                    Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ──┐
│                     140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 1 of 10
│                                   COUNTER 1
│    Head Slot: 0 Drop: 1        Slot: 8
│    INPUTS:. . .                    (next screen for counter 1 output settings)
│    Input Signal counts on: Neg Transition    Use Input 1 for Counter enable: No
│
│    Counter 1 Watchdog Time = 0            DEC        (*0.1sec.)
│
│    Output Setpoint 1, Value 1= 0          DEC
│    Output Setpoint 2, Value 2= 0          DEC
│                         Counter Starts or Restarts . . .
│         Input A: 1            Input B:NONE              Input C: NONE
│    Logic function for inputs to START / RESTART Counter: OR
│
│    Freeze Counter's register for PLC update and Switch Outputs off with....
│         Input D:. 6            or Input E:.NONE         or Input F: NONE
│    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
│    Invert Control Inputs . . .                (applies to all five counters)
│    No. 1: NO                  No. 2: NO                 No. 3: NO
│    No. 4: NO                  No. 5: NO                 No. 6: NO
│    No. 7: NO                  No. 8: NO
│                    Page up / down for prev / next screen
└──────────────────────────────────────────────────────────────────────────┘
```

For Outputs

```
  Hex       Dec      Bin       GoTo                                    Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ──┐
│                     140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 2 of 10
│                                   COUNTER 1 (cont.)
│    Head Slot: 0 Drop: 1        Slot: 8
│    OUTPUTS:  . . .                    (Prev Screen for this counter's 1 input settings)
│    WARNING: DO NOT SELECT THE SAME OUTPUT WITH MORE THAN ONE SET POINT!
│
│    Set Point 1 Linked to Output=          NONE        Invert: NO
│
│    Set Point 2 Linked to Output=          6           Invert: NO
│
│    Final Set Point Linked to Output=      1           Invert: NO
│
│    Timed Final Set Point Linked to Output=  NONE      Invert: NO
│
│    Pulse Width for Timed Final Set Point=  0     DEC  (x0.02 sec)
│    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
│    Invert Control Inputs . . .                (applies to all five counters)
│    No. 1: NO                  No. 2: NO                 No. 3: NO
│    No. 4: NO                  No. 5: NO                 No. 6: NO
│    No. 7: NO                  No. 8: NO
│                    Page up / down for prev / next screen
└──────────────────────────────────────────────────────────────────────────┘
```

Figure 19   Modsoft ver. 2.4 configuration dialog (counter 1 example)

Table 10   Modsoft ver. 2.4 configuration dialog terminology explanations (see above)

Term	Meaning
Terms Common to Input & Output Screens:	
F1, F2, F3 Hex, Dec, Bin	Variable entry and display in hex, decimal, binary
F4 Page selection	Selection of the individual counters (10 screen pages)
F7	Opening of YES/NO fields
Input Signal counts on:	"Pos." or "Neg." transition of counter enable input
Input Screen Terms:	
Use Input 1 for Counter enable?	Select Input 1 to enable counter.
Counter x Watchdog Time:	Counting pulse watchdog time setting in 0.1s steps. 0 disables counting pulse monitoring.
Output Setpoint 1/2 Values: –Relative	If relative Output Set Point mode is selected, output Set Point Values are relative to the Final Set Point Value. Requirement for that: E/S > VA1 >= VA2 >= 0.
–Absolute	If absolute Output Set Point mode is selected, this value is absolute. Requirements for that: E/S > VA2 >= VA1 >= 0.
Counter Starts or Restarts	Assignment of up to 3 discrete inputs for load/start (LS) and restart (ST) function control
Logic function for inputs to START/RESTART counter:	Logic function among inputs to Load / Start or Restart the counter.
... Switch Outputs Off	Assignment of up to 3 process inputs to output switch–off (BEA)
Invert Control Inputs...	Select inversion of all discrete inputs (IN1...IN8)
Output Screen Terms:	
Set Point 1 Linked to Output=	Assignment (and optional inversion) of a process output to the first set–point
Set Point 2 Linked to Output=	Assignment (and optional inversion) of a discrete output to the second set–point
Final Set Point Linked to Output=	Assignment (and optional inversion) of a discrete output to the final set–point
Timed Final Set Point=	Assignment (and optional inversion) of a discrete output to the timed final set–point
Pulse Width for Timed Final Set Point=	Setting of the timed final set–point pulse width (0...255). 0 disables the output.
Invert Control Inputs...	Select inversion of all discrete inputs (IN1...IN8)

Chapter 3
Configuration Examples

- Example 1: Event Counter (Up) with parallel Set Point output activation (counter 1, operatig mode 1)
- Example 2: Repetetive Counter (Up) with serial Set Point output activation (counter 2, operating mode 5)
- Example 3: Differential Counter (Down) with parallel Set Point output activation (counter 3 and 4, operating mode 3)
- Example 4: Event Counter (Up, absolute) with Timed Set Point output activation (counter 4, operating mode A)

☞ **Note:** For all examples the configuration order is as follow:

- Hardware Setup
- Schematic for counter
- Software Settings using Concept
- Software Settings using Modsoft
- Configuration and Start Counter
- Timing Diagram

3.1 Example 1: Event Counter (Up) with parallel Set Point output activation, counter 1, mode 1

3.1.1 Specifications

This application describes using the counter as an event counter 1 in operating mode 1, counting up to 30 counts. See the following specification for counter 1.

Setpoint	Linked Outputs	Active Level	Values
FSP	03	1 –> 0	30 counts
1SP	01	1 –> 0	11 counts
2SP	02	1 –> 0	5 counts
TFSP	04	0 –> 1 (400 ms)	

☞ **Note:**   The values for the Set Points are in relative mode.

☐ Input Pulse is 24V, not inverted.

☐ A Field Signal is connected to input 8 and forces output switch–off.

☐ Input 1 is selected to enable the counter.

☐ The OR logic for the inputs sets the counter.

☐ Watchdog timer is shut off.

☐ IN6 is used to Load / Start, Restart counter.

☐ If communication is lost, the counter outputs will be set to 0.

3.1.2 Hardware Setup

Install the EHC 105 module into the local backplane's slot 8 and secure it, install the module terminal strip and connect an external 24 VDC supply voltage (+ pin 40/– pin 39).

Connect the Pulse input signal to pin 11 (24VDC)

☐ Module wiring can be found on the next page:

Figure 20   Wiring for example 1, event counter

3.1.3   Schematic for Example 1, Event Counter
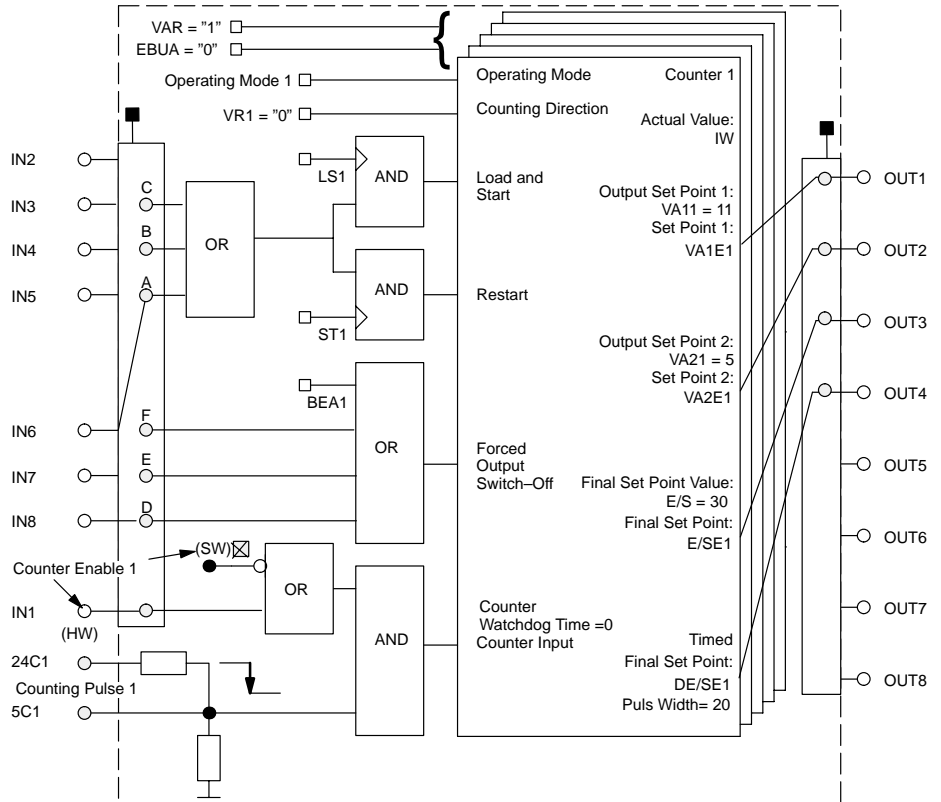
Figure 21   Circuit diagramm

⚠ **Caution: Do not use outputs OUT1...OUT4 with other counters, as such multiple useage is prohibited.**

3.1.4 Software Settings using Concept

I / O Map screen

Local Quantum Drop

Drop
Modules: 5   Bits In: 224 Bits Out: 240
Status Table: ASCII Port none ▾

Module
Bits In: 192   Bits Out: 208
Delete   Params...

Clear	Prev	Next		Cut	Copy	Paste

Slot	Module	Detected	In Ref	In End	Out Ref	Out End	Des ▲
1	CPS 214 00						DC PS 24V
2	CPU x13 0x						CPU 1xMB
3	DDI 353 00		100001	100032			DC IN 24V
4	DDO 353 00				000001	000032	DC OUT 2
5	...						
6	...						
7	...						
8	EHC 105 00		300100	300111	400100	400112	HIGH SPEE
9	...						
10	...						
11	...						
12	...						
13							▼

OK	Cancel	Help	☐ Poll

Counter 1 I/O configuration

140 EHC 105 00

Inversion of Inputs
☐ No. 1   ☐ No. 2   ☐ No. 3   ☐ No. 4   ☐ No. 5   ☐ No. 6   ☐ No. 7   ☐ No. 8

Counter

Counter: 1 ▾

☐ Invert Counter   ☒ Input No. 1 for Counter Enable
Counter Watchdog Time (x 0.1s):   0

Preceded Setpoint
Value 1: 11   Value 2: 5

Inputs
Load/Start or Restart
Logic Between Start Inputs   OR ▾
Input No: 6 ▾   Input No: – ▾   Input No: – ▾

Outputs Switch–Off
Input No: 8 ▾   Input No: – ▾   Input No: – ▾

Outputs

Preceded Signal 1
Output No: 1 ▾   ☐ Invert

Preceded Signal 2
Output No: 2 ▾   ☐ Invert

Final Signal
Output No: 3 ▾   ☐ Invert

Dynamic Final Signal
Output No: 4 ▾   ☐ Invert

Pulse Width (x 0.02 s): 20

OK	Cancel	Help

3.1.4.1   I / O Configuration (see above)

You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Counting pulse 1 with falling edge: no inversion (no cross), active–high.
   ☐ Counter Watchdog Time (x0,1s) = 0.

☐ Counter enable assignment to IN1:
   ☐ Input No.1 for counter enable is selected (cross).

☐ Load/start or restart and output switch–off assignments:
   ☐ Logic Between Start Inputs: OR.
   ☐ Enter IN6 as load/start or restart input, no inversion (no cross).
   ☐ Enter IN8 as output switch–off, no inversion (no cross).

☐ Output assignments, features (dialog screen):
   ☐ Enter OUT1 for Preceded Signal 1, no inversion (no cross).
   ☐ Enter OUT2 for Preceded Signal 2, no inversion (no cross).
   ☐ Enter OUT3 for Final Signal, no inversion (no cross).
   ☐ Enter OUT4 for Dynamic Final Signal, no inversion (no cross).
   ☐ Dynamic Final Signal Pulse Width (x0,02 s) = 20.

☞ **Note:**   Check the other counters with their default output assignement, because multiple usage is prohibited.

☐ Enter the first and second Preceded Setpoint:
–Preceded Set Points, value 1 = 11, value 2 = 5 .

3.1.4.2   Configuration of Final Signal Value and counter characteristics

From the Data Reference Screen, select the 4x – register, (defined on page 49)(I/O Map screen) and specify Set Point Value.

☐ Specify Final Signal Value:
   ☐ Enter the Final Signal Value (E/S) as 32–bit value (with user program):
    –E/S1: 400103 = 30 LD (see also page 31) (Output structure).

☐ Specify counter characteristics:
   ☐ Enter parallel event counter (0001), counting up (0000),
    relative Set Point (0001), (with user program):
    –400100 – register = 1010 **hex (**see also page 31**)** (Output structure).

3.1.5 Software Settings using Modsoft

I / O Map screen

```
┌─────────────────────────────────────────────────────────────────┐
│ Utility        ClrDrop  HoldTime  ASCPort Drop      QUANTUM              Quit │
│ F1 ── F2 ── F3 ── F4 ── F5 ── F6 ── F7−Lev 8−F8−OFF ── F9 ──  │
│                        QUANTUM I/O MAP                            │
│   Type:  Local I/O          Head−Slot: 0      Drop:  1      Available:  444   │
│   Drop Hold Up Time :  3  x100ms     Module Status Reg:  0        │
│   Number of Inputs :   192              Number of Outputs :   208 │
│  ─────────────────────────────────────────────────────────────  │
│   Slot        Module        Input Ref        Ourput Ref      Description   │
│   101                                                            │
│   102                                                            │
│   103                                                            │
│   104                                                            │
│   105                                                            │
│   106                                                            │
│   107                                                            │
│   108     ▌EHC 105 00▐   300100−300111  400100−400112  EHC10500 High Speed │
│   109                                                            │
│   110                                                            │
│   111                                                            │
│   112                                                            │
│   113                                                            │
│                                                                  │
└─────────────────────────────────────────────────────────────────┘
```

Figure 22   Configuration under Modsoft

3.1.5.1   I / O Configuration (see below)
You must stop the controller before configuring the module.

Use the following selection to configure the counter.

□ Input Signal counts on: neg. transition.
□ Counter 1 Watchdog Time (x0,1sec) = 0
□ Counter enable assignment to IN1, (dialog screen 1):
   □ Use Input1 for counter enable: Yes.
□ Load/start or restart and output switch–off assignments,(dialog screen 1):
   □ Logic function for inputs to Start / Restart Counter: OR.
   □ Enter IN6 as Starts or Restarts Counter, no inversion.
   □ Enter IN8 as Freeze Counter's register for PLC update and Switch
     Outputs off with..., (no inversion of IN8).
□ Enter the first and second output Set Points (dialog screen 1)
  –Output Set Points, value 1 = 11, value 2 = 5 .
□ Output assignments, (dialog screen 2):
   □ Enter OUT1 for Set Point 1, no inversion.
   □ Enter OUT2 for Set Point 2, no inversion.
   □ Enter OUT3 for Final Set Point, no inversion.
   □ Enter OUT4 for Timed Final Set Point, no inversion.
   □ Enter Pulse Width for Timed Final Set Point (x0,02 sec) = 20.

☞ **Note:** Check the other counters with their default output assignement, because multiple usage is prohibited.

Counter 1 I/O Configuration
For Inputs

```
Hex        Dec      Bin       GoTo                                      Quit
F1 —— F2 —— F3 —— F4  I / O Map Module Editor · F7−Lev 8−F8−OFF —— F9 ——
               140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 1 of 10
                              COUNTER 1
   Head Slot: 0 Drop: 1        Slot: 8
   INPUTS:. . .                    (next screen for counter 1 output settings)
   Input Signal counts on: Neg Transition    Use Input 1 for Counter enable: Yes

   Counter 1 Watchdog Time = 0              DEC       (*0.1sec.)

   Output Setpoint 1, Value 1= 11           DEC
   Output Setpoint 2, Value 2=5             DEC
                         Counter Starts or Restarts . . .
      Input A: 6              Input B:NONE              Input C: NONE
   Logic function for inputs to START / RESTART Counter: OR

   Freeze Counter's register for PLC update and Switch Outputs off with....
      Input D:. 8           or Input E:.NONE           or Input F: NONE
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   Invert Control Inputs . . .                 (applies to all five counters)
   No. 1: NO                    No. 2: NO                    No. 3: NO
   No. 4: NO                    No. 5: NO                    No. 6: NO
   No. 7: NO                    No. 8: NO
                    Page up / down for prev / next screen
```

For Outputs

```
Hex        Dec      Bin       GoTo                                      Quit
F1 —— F2 —— F3 —— F4  I / O Map Module Editor · F7−Lev 8−F8−OFF —— F9 ——
               140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 2 of 10
                            COUNTER 1 (cont.)
   Head Slot: 0 Drop: 1        Slot: 8
   OUTPUTS: . . .                    (Prev Screen for this counter's 1 input settings)
   WARNING: DO NOT SELECT THE SAME OUTPUT WITH MORE THAN ONE Set Point!

   Set Point 1 Linked to Output=          1              Invert: NO

   Set Point 2 Linked to Output=          2              Invert: NO

   Final Set Point Linked to Output=      3              Invert: NO

   Timed Final Set Point Linked to Output=  4            Invert: NO

   Pulse Width for Timed Final Set Point=   20     DEC   (x0.02 sec)
- - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   Invert Control Inputs . . .       (applies to all five counters)
   No. 1: NO                    No. 2: NO                    No. 3: NO
   No. 4: NO                    No. 5: NO                    No. 6: NO
   No. 7: NO                    No. 8: NO
                    Page up / down for prev / next screen
```

Figure 23   Modsoft dialog screen

3.1.5.2   Configuration of Final Set Point Value and counter characteristics
(see above)
From the Data Reference Screen for this counter select the 4x – registers,
(defined in Figure 22 on page 51) and specify Set Point Value.

☐ Specify Set Point Value:
☐ Enter the Final Set Point Value (E/S) as 32–bit value (with user program):
  –E/S1: 400103 = 30 LD (see also page 31)

☐ Specify counter characteristics as:
☐ Enter parallel event counter (0001), counting up (0000),
  relative Set Point (0001), (with user program):
  –400100 – register = 1010 **hex (**see also page 31**)**

3.1.6   Start Counter 1

Start the controller, then from module data reference screen:

Step 1   Load/start counter:
–Activate (High) discrete input 6 (pin 26) .
–Enter LS1 bit in 400100 – register (D8 = "1" resp. 1110 hex) (with user
program), (see also page 31) (Output structure).

Effect   The outputs switch to "1" signal and the counter's actual value is set to 0:
–300101 – register:
    VA1E1(D0) = OUT1 = "1" signal
    VA2E1(D8) = OUT2 = "1" signal
–300100 – register:
    E/SE1(D8) = OUT3 = "1" signal;
–300102 –register:
    counter's actual value = 0

Step 2   Enter "1" signal on discrete input IN1 (pin 21, counter enable). This enables
the counter 1.

Effect   Counter 1 counts the pulses at counter input 1:
–at actual value 19 = 30–11 OUT1 switches off,
–at actual value 25 = 30–5 OUT2 switches off,
–at actual value 30 OUT3 switches off and
–the Timed Final Set Point (Dynamic Final Signal) output OUT4 switches on
for 400 ms.

If the counter has not reached the Final Set Point Value (Final Signal Value), the
outputs OUT1 .. OUT4 can be switched off with an external "1" signal connected
to input IN8 or through the 400100 – register BEA1 bit (with D10 = "1" resp.
1410 hex, since the operating mode must be retained). All outputs and the input

status word bits (300100 – register (D8), 300101–register (D0 and D8)) switches to "0" signal. See also page 13, Figure 5 Relationship diagram.

A restart is possible through discrete input IN6 and a rising edge at the 400100 – register ST1 bit (D9, resp. 1210 hex), provided that the Final Set Point Value (actual value 30 in our example) has not been reached.
You can Restart only after output switch–off (BEA). Refer to page 12 Relationship diagram.

3.1.7   Example 1 Timing Diagram

Counter Input (clock Input) 1 (24C1)   Pulse Generator Pulses

Load and Start / Restart (IN6)

LS1

(HW) Counter (Clock) Enable (IN1)

Actual Value IW1

E/S1 Value

VA21 Value
VA11 Value

0

VA1E1 (OUT1)

VA2E1 (OUT2)   Counter Outputs

E/SE1 (OUT3)

DE/SE1 (OUT4)

Counter Actual Value

5

11

30

DE/SE1 pulse width can be specified in the Concept/Modsoft dialog screen
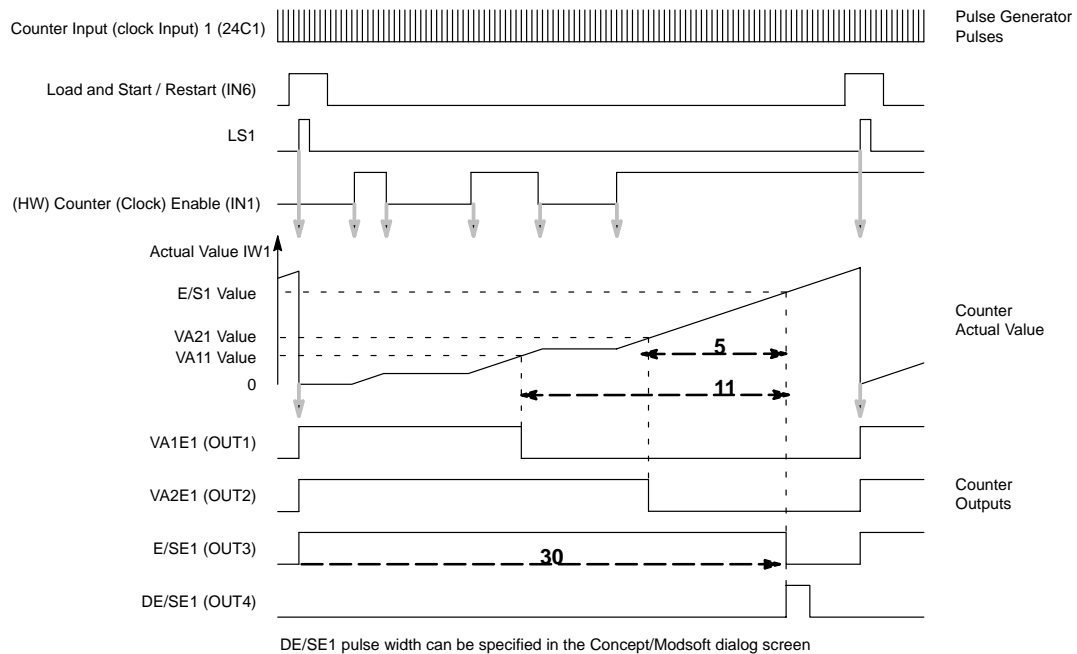
Figure 24   Event counter with parallel output activation (up)

☞ **Note:**   If pulses continue to appear at counter input 1 after reaching the Final Set Point Value (30), the pulses will also be counted and displayed as the current actual value in the 300102– register as a 32–bit value.

54   Configuration Examples

When the counter is reset (Load/Start) the counting value is set to 0 and the outputs became active again.

Note: If the counter's operating mode, counting direction, switch–off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

3.2 Example 2: Repetitive Counter (Up) with serial setpoint output activation, counter 2, mode 5

3.2.1 Specifications

This application describes using the counter 2 as an repetitive counter with serial setpoint output activation counter 2, mode 5, counting up to 30 counts. See the following specification for counter 2.

Setpoint	Linked Outputs	Active Level	Values
FSP	03	1 –> 0	30 counts
1SP	01	1 –> 0	11 counts
2SP	02	1 –> 0	5 counts
TFSP	04	0 –> 1 (400 ms)	

☞ **Note:** The values for the Set Points are in relative mode.

☐ Input Pulse is 24V, not inverted.

☐ A Field Signal is connected to input 8 and forces output switch–off.

☐ Input 2 is not selected to enable the counter.

☐ The OR logic for the inputs sets the counter.

☐ Watchdog timer is shut off.

☐ IN2 is used to Load / Start, Restart counter.

☐ If communication is lost, the counter outputs will be set to 0.

3.2.2 Hardware Setup

Install the EHC 105 module into the local backplane's slot 8 and secure it. Install the module terminal strip and connect an external 24 VDC supply voltage (+ pin 40/– pin 39).

Connect the Pulse input signal to pin 13 (24VDC)

☐ Module wiring can be found on the next page:
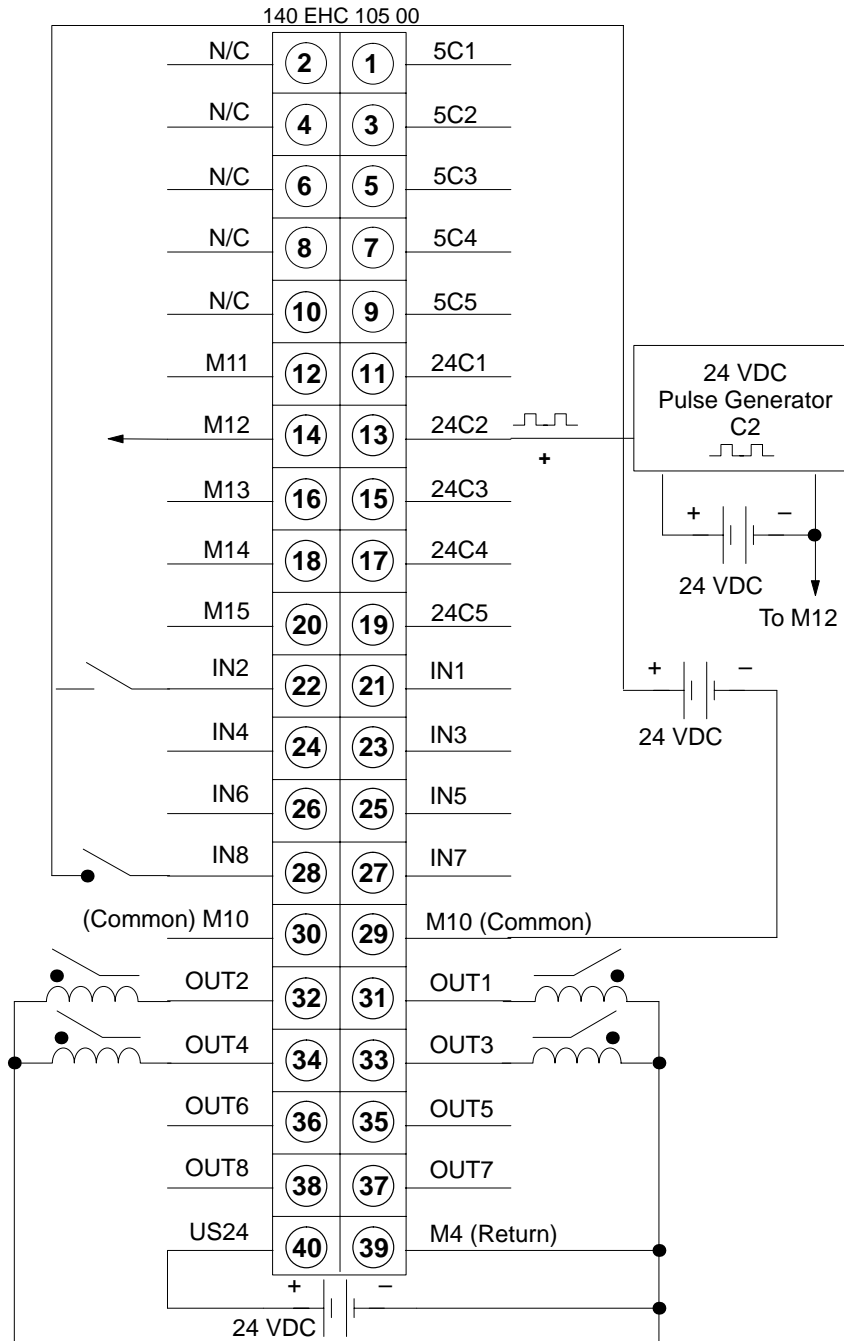
Figure 25   Wiring for example 2, repetitive counter

Configuration Examples   57

3.2.3 Schematic for Example 2, Repetitive Counter
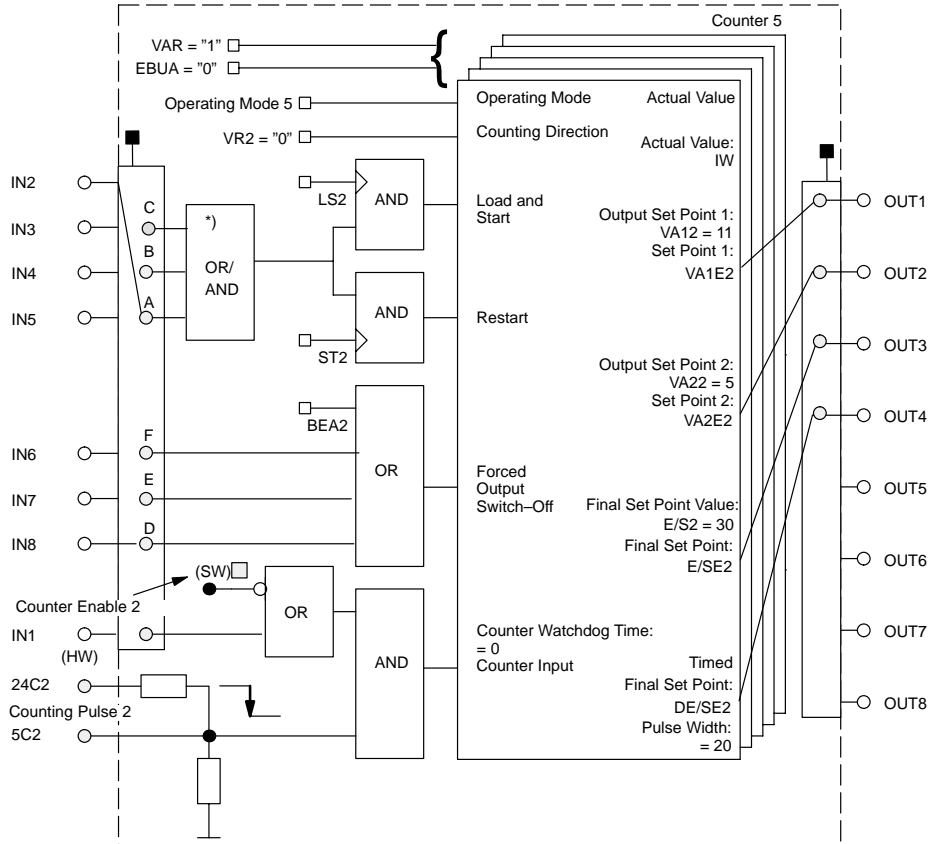
Figure 26   Circuit diagram

⚠ **Caution: Do not use outputs OUT1...OUT4 with other counters, as such multiple useage is prohibited.**

3.2.4 Software Settings using Concept

I / O Map screen (refer to example 1, page 49)

Counter 2 I/O Configuration

```
┌──────────────────────────────────────────────────────────────────────────┐
│ ▬                           140 EHC 105 00                                 │
├──────────────────────────────────────────────────────────────────────────┤
│ ┌─Inversion of Inputs────────────────────────────────────────────────────┐│
│ │ ☐ No. 1   ☐ No. 2   ☐ No. 3   ☐ No. 4   ☐ No. 5   ☐ No. 6   ☐ No. 7   ☐ No. 8 ││
│ └────────────────────────────────────────────────────────────────────────┘│
│ ┌─Counter────────────────────────────────────┐┌─Outputs──────────────────┐│
│ │          Counter: [2  ⯯]                    ││ ┌─Preceded Signal 1──────┐││
│ │                                             ││ │ Output No: [1  ⯯] ☐ Invert│││
│ │ ┌────────────────────────────────────────┐ ││ └────────────────────────┘││
│ │ │ ☐ Invert Counter  ☐ Input No. 2 for Counter Enable ││ ┌─Preceded Signal 2──────┐││
│ │ │ Counter Watchdog Time (x 0.1s):  [0  ] │ ││ │ Output No: [2  ⯯] ☐ Invert│││
│ │ └────────────────────────────────────────┘ ││ └────────────────────────┘││
│ │ ┌─Preceded Setpoint──────────────────────┐ ││ ┌─Final Signal───────────┐││
│ │ │ Value 1: [11   ]   Value 2: [5   ]     │ ││ │ Output No: [3  ⯯] ☐ Invert│││
│ │ └────────────────────────────────────────┘ ││ └────────────────────────┘││
│ │ ┌─Inputs─────────────────────────────────┐ ││ ┌─Dynamic Final Signal───┐││
│ │ │ ┌─Load/Start or Restart──────────────┐ │ ││ │ Output No: [4  ⯯] ☐ Invert│││
│ │ │ │ Logic Between Start Inputs [OR  ⯯] │ │ ││ └────────────────────────┘││
│ │ │ │ Input No: [2 ⯯] Input No: [– ⯯] Input No: [– ⯯] │ ││                          ││
│ │ │ └────────────────────────────────────┘ │ ││ Pulse Width (x 0.02 s): [20]││
│ │ │ ┌─Outputs Switch–Off─────────────────┐ │ ││                          ││
│ │ │ │ Input No: [8 ⯯] Input No: [– ⯯] Input No: [– ⯯] │ ││                          ││
│ │ │ └────────────────────────────────────┘ │ ││                          ││
│ │ └────────────────────────────────────────┘ │└──────────────────────────┘│
│ └────────────────────────────────────────────┘                            │
│ ┌──────────────┐          ┌──────────────┐          ┌──────────────┐      │
│ │      OK      │          │    Cancel    │          │     Help     │      │
│ └──────────────┘          └──────────────┘          └──────────────┘      │
└──────────────────────────────────────────────────────────────────────────┘
```

3.2.4.1   I / O Configuration (see above)
You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Counting pulse 2 with falling edge: no inversion (no cross), active–high.
  ☐ Counter Watchdog Time (x0,1s) = 0.

☐ Input 2 For Counter Enable is not selected (no cross) .

☐ Load/start or restart and output switch–off assignments:
  ☐ Logic Between Start Inputs: OR.
  ☐ Enter IN2 as load/start or restart input, no inversion (no cross).
  ☐ Enter IN8 as output switch–off, no inversion (no cross).

☐ Output assignments, features (dialog screen):
  ☐ Enter OUT1 for Preceded Signal 1, no inversion (no cross).
  ☐ Enter OUT2 for Preceded Signal 2, no inversion (no cross).
  ☐ Enter OUT3 for Final Signal, no inversion (no cross).
  ☐ Enter OUT4 for Dynamic Final Signal, no inversion (no cross).

□ Dynamic Final Signal Pulse Width (x0,02 s) = 20.

☞ **Note:** Check the other counters with their default output assignement, because multiple usage is prohibited.

□ Enter the first and second Preceded Setpoint:
  –Preceded Set Points, value 1 = 11, value 2 = 5 .

3.2.4.2 Configuration of Final Signal Value and counter characteristics
(see above)
From the Data Reference Screen for this counter select the 4x – register, (defined on page 49)(I/O Map screen) and specify Set Point Value.

□ Specify Final Signal Value:
  □ Enter the Final Signal Value (E/S) as 32–bit value (with user program):
    –E/S2: 400105 = 30 LD (see also page 31) (Output structure).
□ Specify counter characteristics:
  □ Enter repetitive counter (0101), counting up (0000):
    –400101 – register = 00**5**0 **hex** (mode) (see also page 31),
    relative Set Point (0001), (with user program):
    –400100 – register = 00**1**0 **hex** (relative).

3.2.5 Software Settings using Modsoft

I / O Map screen (refer to example 1, page 51)

Counter 2 I/O Configuration

For Inputs

```
  Hex        Dec      Bin        GoTo                                      Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ─┐
│                140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 3 of 10 │
│                               COUNTER 2                                   │
│    Head Slot: 0 Drop: 1        Slot: 8                                    │
│    INPUTS:. . .                   (next screen for counter 2 output settings)│
│    Input Signal counts on: Neg Transition    Use Input 2 for Counter enable: NO│
│                                                                          │
│    Counter 2 Watchdog Time = 0            DEC        (*0.1sec.)           │
│                                                                          │
│    Output Setpoint 1, Value 1=11          DEC                            │
│    Output Setpoint 2, Value 2=5           DEC                            │
│                        Counter Starts or Restarts . . .                  │
│       Input A: 2            Input B:NONE              Input C: NONE       │
│    Logic function for inputs to START / RESTART Counter: OR              │
│                                                                          │
│    Freeze Counter's register for PLC update and Switch Outputs off with....│
│       Input D:. 8         or Input E:.NONE           or Input F: NONE     │
│    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -│
│    Invert Control Inputs . . .           (applies to all five counters)  │
│    No. 1: NO               No. 2: NO                No. 3: NO             │
│    No. 4: NO               No. 5: NO                No. 6: NO             │
│    No. 7: NO               No. 8: NO                                      │
│                   Page up / down for prev / next screen                  │
└──────────────────────────────────────────────────────────────────────┘
```

For Outputs

```
  Hex        Dec      Bin        GoTo                                      Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ─┐
│                140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 4 of 10 │
│                            COUNTER 2 (cont.)                             │
│    Head Slot: 0 Drop: 1        Slot: 8                                    │
│    OUTPUTS:  . . .              (Prev Screen for this counter's 2 input settings)│
│    WARNING: DO NOT SELECT THE SAME OUTPUT WITH MORE THAN ONE SET POINT!  │
│                                                                          │
│    Set Point 1 Linked to Output=          1           Invert: NO         │
│                                                                          │
│    Set Point 2 Linked to Output=          2           Invert: NO         │
│                                                                          │
│    Final Set Point Linked to Output=      3           Invert: NO         │
│                                                                          │
│    Timed Final Set Point Linked to Output=  4         Invert: NO         │
│                                                                          │
│    Pulse Width for Timed Final Set Point=  20    DEC   (*0.02):          │
│    - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -│
│    Invert Control Inputs . . .           (applies to all five counters)  │
│    No. 1: NO               No. 2: NO                No. 3: NO             │
│    No. 4: NO               No. 5: NO                No. 6: NO             │
│    No. 7: NO               No. 8: NO                                      │
│                   Page up / down for prev / next screen                  │
└──────────────────────────────────────────────────────────────────────┘
```

Figure 27   Modsoft I/O configuration

3.2.5.1 I / O Configuration (see above)

You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Input Signal counts on: neg. transition.
　☐ Counter 2 Watchdog Time (x0,1sec) = 0

☐ Counter enable assignment to IN2, (dialog screen 3):
　☐ Use Input 2 for counter enable: No

☐ Load/start or restart and output switch–off assignments,(dialog screen 3):
　☐ Logic function for inputs to Start / Restart Counter: OR.
　☐ Enter IN2 as Counter Starts or Restarts, no inversion.
　☐ Enter IN8 as Freeze Counter's register for PLC update and Switch Outputs off with..., (no inversion IN8).

☐ Enter the first and second output Set Points (dialog screen 3)
　–Output Set Points, value 1 = 11, value 2 = 5 .

☐ Output assignments, (dialog screen 4):
　☐ Enter OUT1 for Set Point 1, no inversion.
　☐ Enter OUT2 for Set Point 2, no inversion.
　☐ Enter OUT3 for Final Set Point, no inversion.
　☐ Enter OUT4 for Timed Final Set Point, no inversion.
　☐ Enter Pulse Width for Timed Final Set Point (x0,02 sec) = 20.

☞ **Note:**　Check the other counters with their default output assignement, because multiple usage is prohibited.

3.2.5.2 Configuration of Final Set Point Value and counter characteristics
(see above)

From the Data Reference Screen for this counter, select the 4x – register (defined in Figure 22 on page 51) and specify Set Point Value.

☐ Specify Set Point Value:
　☐ Enter the Final Set Point Value (E/S) as 32–bit value (with user program):
　　–E/S2: 400105 = 30 LD (see also page 31)

☐ Specify counter characteristics as:
　☐ Enter repetetive counter (0101), counting up (0000):
　　–400101 – register = 00**5**0 **hex** (mode)**,**　(see also page 31),
　　relative Set Point (0001), (with user program):
　　–400100 – register = 00**1**0 **hex** (relative).

3.2.6 Start Counter 2

Start the controller, then from module data reference screen:

Step 1 Load/start counter:
–Activate (High) discrete input 2 (pin 22) .
–Enter LS2 bit in 400101 – register (D0 = "1" resp. 00**51 hex)** (with user
program), (see also page 31) (Output structure).

Effect The outputs switch to "1" signal and the counter's actual value is set to 0:
–300101 – register:
VA1E2(D1) = OUT1 = "1" signal
VA2E2(D9) = OUT2 = "0" signal
–300100 – register:
E/SE2 (D9) = OUT3 = "0" signal;
–300104 –register:
counter's actual value = 0

☞ **Note:** The counter input is inherently enabled, as there has been no discrete
input assigned.

Effect Counter 2 counts the pulses at counter input 2:
–at actual value 19 = 30–11 OUT1 switches off and the OUT2 switches on,
–at actual value 25 = 30–5 OUT2 switches off and the OUT3 switches on,
–at actual value 30 OUT3 switches off and OUT1 switches on and
–the Timed Final Set Point (Dynamic Final Signal) output OUT4 switches on
 for 400 ms and
–the counters actual value is set to 0 and
–the counting procedure repeats.

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3.2.7   Example 2 Timing Diagram

DE/SE2 pulse width can be specified in the Concept/Modsoft dialog screen
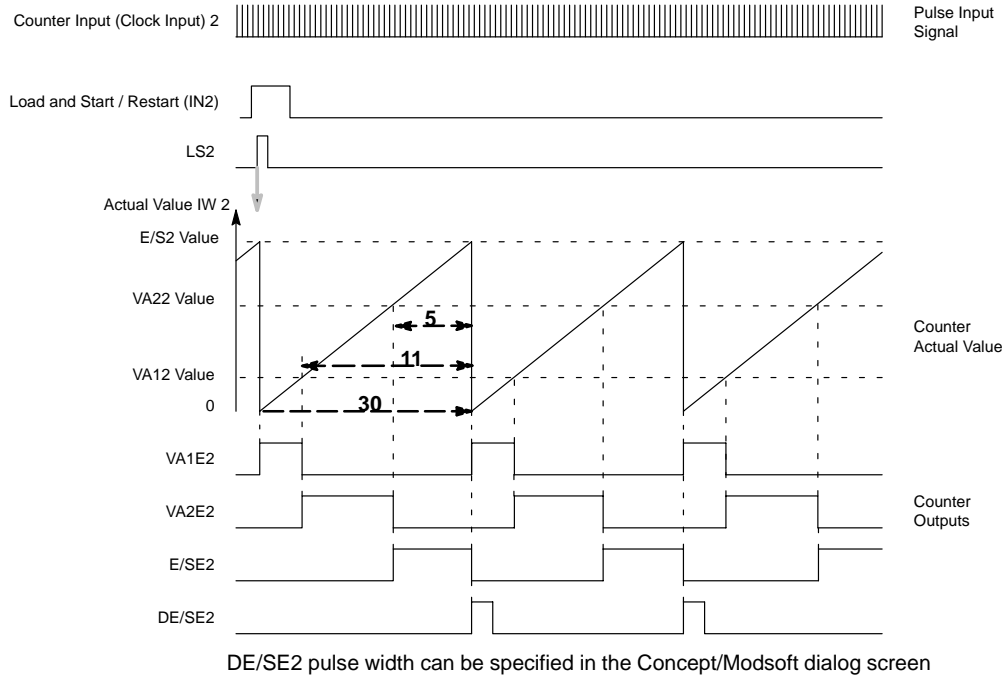
Figure 28   Repetitive counter

☞ **Note:**   The output set points are relative to terminal value E/S = 30.

☞ **Note:**   A restart through discrete input IN2 and the ST2 bit in the 4x +1 – register = 0052 hex (D1) with rising edge is not possible in this operating mode.

☞ **Note:**   OUT1 .. OUT4 can be switched off with an external "1" signal connected to input IN8 or through the 400101 – register BEA2 bit (with D2 = "1" resp. 0054 hex, since the operating mode must be retained). This means all outputs and the input status word bits (300100 – register (D9), 300101–register (D1 and D9)) switche to "0" signal. See also page 13, Figure 5 Relationship diagram.

☞ **Note:**   If the counter's operating mode, counting direction, switch–off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

3.3 Example 3: Differential Counter (Down) with parallel Set Point output activation, mode 3

3.3.1 Specifications

This application describes using counter 3 and 4 as a differential counter with parallel Set Point output activation, counting down from 30 to 0. See the following specification for counter 3.

Setpoint	Linked Outputs	Active Level	Values
FSP	03	1 –> 0	30 counts (E/S3)
1SP	01	1 –> 0	11 counts
2SP	02	1 –> 0	5 counts
TFSP	04	0 –> 1 (400 ms)	

☞ **Note:** The values for the Set Points are in relative mode.

☞ **Note:** For this application the FSP is the starting value for the down counter.

☐ Input Pulse is 24V, not inverted.

☐ There is no configuration from the Forced Output Switch–Off logic to a discrete Input.

☐ No counter enable comes from discrete input IN3.

☐ The OR logic for the inputs sets the counter.

☐ Watchdog timer is shut off.

☐ If communication is lost, the counter outputs will be set to 0.

3.3.2 Hardware Setup

Install the EHC 105 module into the local backplane's slot 8 and secure it. Install the module terminal strip and connect an external 24 VDC supply voltage (+ pin 40/– pin 39).

Connect the Pulse input signal from two pulse generators to pin 15 and 17 (24VDC)

□ Module wiring can be found on page 66:

140 EHC 105 00

N/C	2	1	5C1
N/C	4	3	5C2
N/C	6	5	5C3
N/C	8	7	5C4
N/C	10	9	5C5
M11	12	11	24C1
M12	14	13	24C2
M13	16	15	24C3
M14	18	17	24C4
M15	20	19	24C5
IN2	22	21	IN1
IN4	24	23	IN3
IN6	26	25	IN5
IN8	28	27	IN7
(Common) M10	30	29	M10 (Common)
OUT2	32	31	OUT1
OUT4	34	33	OUT3
OUT6	36	35	OUT5
OUT8	38	37	OUT7
US24	40	39	M4 (Return)

To M13

24 VDC

24 VDC
Pulse Generator
C3

24 VDC
Pulse Generator
C4

24 VDC

To M14

24 VDC
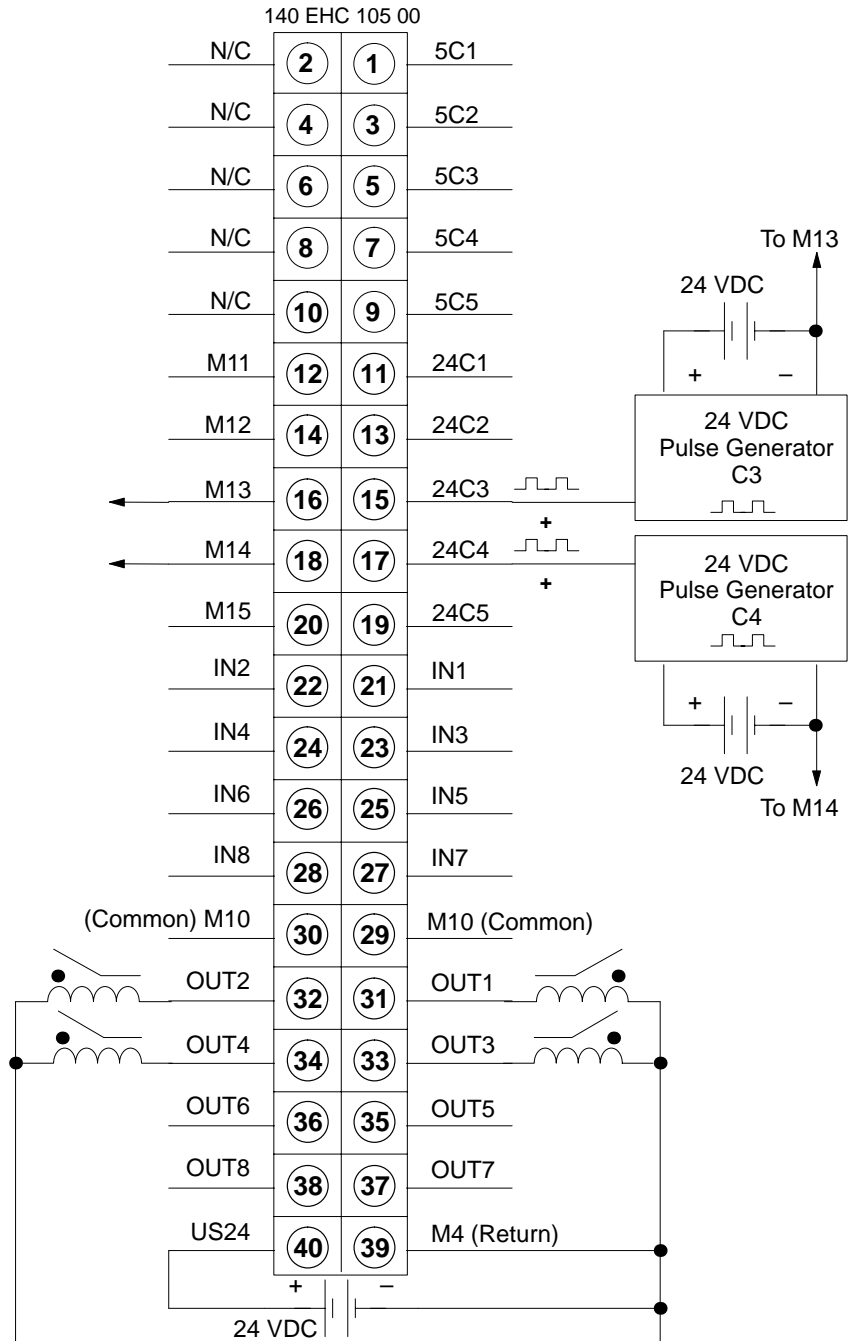
Figure 29   Wiring for example 3, differential counter

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3.3.3 Schematic for Example 3, Differential Counter
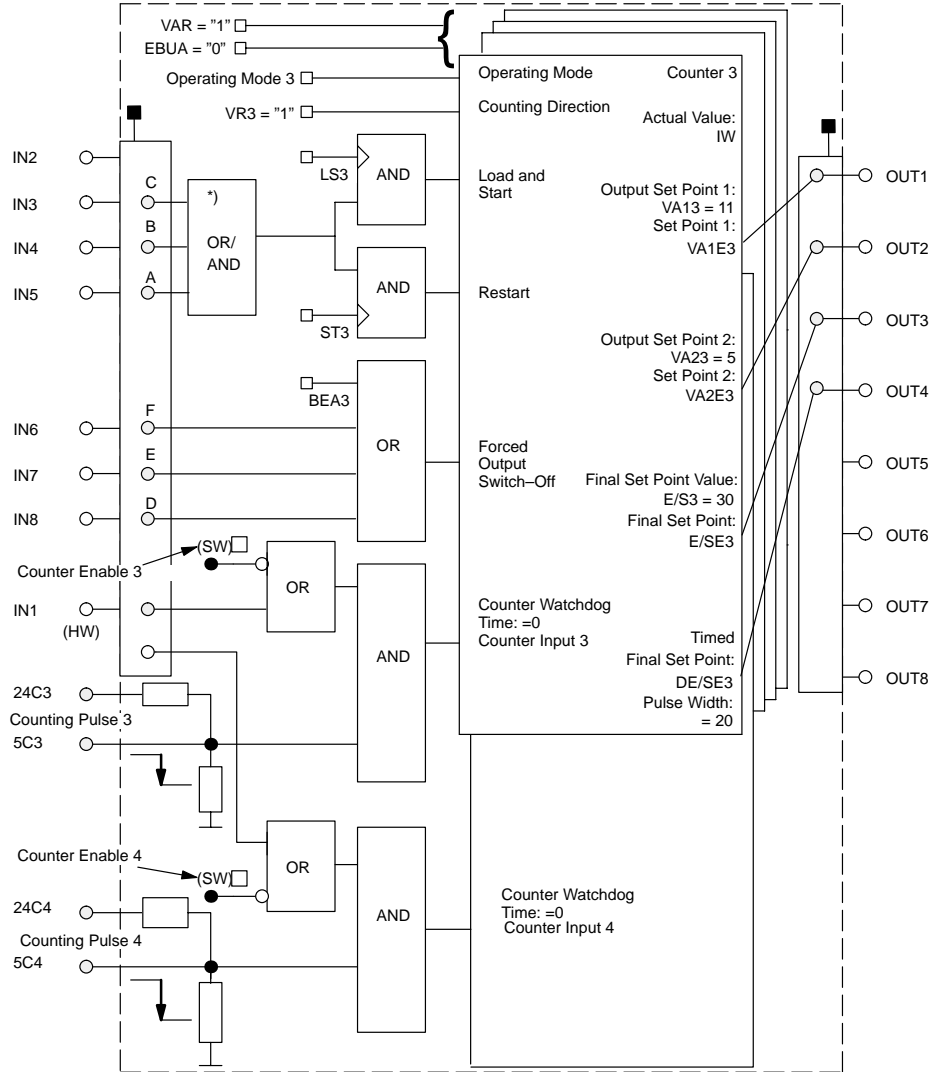
Figure 30   Circuit diagram

⚠️ **Caution: Do not use outputs OUT1...OUT4 with other counters, as such multiple useage is prohibited.**

👉 **Note:**   The differential counter consists of counter 3 and 4. For this application, counter 3 is the master and its configuration also applies to counter 4. The input and output asignements, Watchdog Time and the Set Point values for counter 4

were ignored.

3.3.4 Software Settings using Concept

I / O Map screen (refer to example 1, page 49)

Counter 3 I/O Configuration

```
┌─────────────────────────────────────────────────────────────────────────────┐
│ ▬                            140 EHC 105 00                                   │
├─────────────────────────────────────────────────────────────────────────────┤
│ ┌─Inversion of Inputs──────────────────────────────────────────────────────┐ │
│ │ ☐ No. 1    ☐ No. 2    ☐ No. 3    ☐ No. 4    ☐ No. 5    ☐ No. 6   ☐ No. 7   ☐ No. 8 │ │
│ └──────────────────────────────────────────────────────────────────────────┘ │
│ ┌─Counter─────────────────────────────────────┐ ┌─Outputs──────────────────┐ │
│ │         Counter: 3   ⬇                       │ │ ┌─Preceded Signal 1────┐ │ │
│ │                                              │ │ │ Output No: 1  ⬇ ☐ Invert│ │
│ │  ☐ Invert Counter  ☐ Input No. 3 for Counter Enable │ └──────────────────┘ │ │
│ │  Counter Watchdog Time (x 0.1s):      0      │ │ ┌─Preceded Signal 2────┐ │ │
│ │ ┌─Preceded Setpoint─────────────────────┐    │ │ │ Output No: 2  ⬇ ☐ Invert│ │
│ │ │ Value 1: 11          Value 2: 5        │    │ │ └──────────────────┘ │ │
│ │ └───────────────────────────────────────┘    │ │ ┌─Final Signal────────┐ │ │
│ │ ┌─Inputs─────────────────────────────────┐   │ │ │ Output No: 3  ⬇ ☐ Invert│ │
│ │ │┌─Load/Start or Restart───────────────┐ │   │ │ └──────────────────┘ │ │
│ │ ││ Logic Between Start Inputs  OR   ⬇ │ │   │ │ ┌─Dynamic Final Signal─┐ │ │
│ │ ││Input No: ─ ⬇ Input No: ─ ⬇ Input No: ─ ⬇│ │ │ │ Output No: 4  ⬇ ☐ Invert│ │
│ │ │└─────────────────────────────────────┘ │   │ │ └──────────────────┘ │ │
│ │ │┌─Outputs Switch–Off──────────────────┐ │   │ │                         │ │
│ │ ││Input No: ─ ⬇ Input No: ─ ⬇ Input No: ─ ⬇│ │ │ Pulse Width (x 0.02 s): 20│ │
│ │ │└─────────────────────────────────────┘ │   │ └──────────────────────────┘ │
│ └────────────────────────────────────────────┘                               │
│                                                                               │
│ ┌──── OK ────┐        ┌──── Cancel ────┐            ┌──── Help ────┐          │
│ └────────────┘        └────────────────┘            └──────────────┘          │
└─────────────────────────────────────────────────────────────────────────────┘
```

3.3.4.1   I / O Configuration Counter 3 (see above)
You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Counting pulse 3 with falling edge: no inversion (no cross), active–high.
  ▫ Counter Watchdog Time (x0,1s) = 0.

☐ Input 3 for Counter Enable ist not selected (no cross).

☐ Load/start or restart and output switch–off assignments:
  ▫ Logic Between Start Inputs: OR.
  ▫ There is no Input selected for load/start or restart counter.
  ▫ There is no Input selected for output switch–off.

☐ Output assignments, features (dialog screen):
  ▫ Enter OUT1 for Preceded Signal 1, no inversion (no cross).

□ Enter OUT2 for Preceded Signal 2, no inversion (no cross).
□ Enter OUT3 for Final Signal, no inversion (no cross).
□ Enter OUT4 for Dynamic Final Signal, no inversion (no cross).
□ Dynamic Final Signal Pulse Width (x0,02 s) = 20.

☞ **Note:** Check the other counters with their default output assignement, because multiple usage is prohibited.

□ Enter the first and second Preceded Setpoint:
  –Preceded Set Points, value 1 = 11, value 2 = 5 .

3.3.4.2 Configuration of Final Signal Value and counter characteristics for Counter 3 (see above)
From the Data Reference Screen for this counter select the 4x – register, (defined on page 49)(I/O Map screen) and specify Set Point Value.

□ Specify Final Signal Value:
  □ Enter the Final Signal Value (E/S) as 32–bit value (with user program):
    –E/S3: 400107 = 30 LD (see also page 31) (Output structure).
□ Specify counter characteristics:
  □ Enter parallel differential counter (0011), counting down (1000):
    –400101 – register = 3800 **hex**,
    relative Set Point (0001), (with user program):
    –400100 – register = 00**1**0 **hex** (see also page 31) (Output structure).

⚠ **Caution: For counter 4, only the selections ”Invert Counter” and ”Input No. 4 for Counter Enable” are useable. All other assignements were ignored.**

3.3.5 Software Settings using Modsoft

I / O Map screen (refer to example 1, page 51)

Counter 3 I / O Configuration

For Inputs

```
 Hex      Dec     Bin       GoTo                                          Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ─
                140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 5 of 10
                                    COUNTER 3
     Head Slot: 0 Drop: 1        Slot: 8
     INPUTS:. . .                    (next screen for counter 3output settings)
     Input Signal counts on: Neg Transition    Use Input 3 for Counter enable: NO

     Counter 3 Watchdog Time =0              DEC        (*0.1sec.)

     Output Setpoint 1, Value 1= 11          DEC
     Output Setpoint 2, Value 2= 5           DEC
                           Counter Starts or Restarts . . .
         Input A: NONE        Input B:NONE              Input C: NONE
     Logic function for inputs to START / RESTART Counter: OR

     Freeze Counter's register for PLC update and Switch Outputs off with....
        Input D:NONE.        or Input E:.NONE           or Input F: NONE
     - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Invert Control Inputs . . .               (applies to all five count-
     ers)
     No. 1: NO                 No. 2: NO                No. 3: NO
     No. 4: NO                 No. 5: NO                No. 6: NO
     No. 7: NO          Page up / down for prev / next screen
```

For Outputs

```
 Hex      Dec     Bin       GoTo                                          Quit
┌ F1 ── F2 ── F3 ── F4  I / O Map Module Editor · F7−Lev 8−F8−OFF ── F9 ─
                140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 6 of 10
                                    COUNTER 3 (cont.)
     Head Slot: 0 Drop: 1        Slot: 8
     OUTPUTS: . . .                 (Prev Screen for this counter's 3 input settings)
     WARNING: DO NOT SELECT THE SAME OUTPUT WITH MORE THAN ONE SET POINT!

     Set Point 1 Linked to Output=           1            Invert: NO

     Set Point 2 Linked to Output=           2            Invert: NO

     Final Set Point Linked to Output=       3            Invert: NO

     Timed Final Set Point Linked to Output=  4           Invert: NO

     Pulse Width for Timed Final Set Point=   20   DEC   (*0.02):
     - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
     Invert Control Inputs . . .               (applies to all five counters)
     No. 1: NO                 No. 2: NO                No. 3: NO
     No. 4: NO                 No. 5: NO                No. 6: NO
     No. 7: NO                 No. 8: NO
                  Page up / down for prev / next screen
```

Figure 31   Modsoft dialog screen

3.3.5.1   I / O Configuration (see above)
You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Input Signal counts on: neg. transition.
   ☐ Counter 3 Watchdog Time (x0,1sec) = 0

☐ Use Input3 for counter enable: No (dialog screen 1).
☐ Load/start or restart and output switch–off assignments,(dialog screen 1):
   ☐ Logic function for inputs to Start / Restart Counter: OR.
   ☐ There is no Input selected for Starts or Restarts Counter.
   ☐ There is no Input selected for Freeze Counter's register for PLC update
      and Switch Outputs off.

☐ Enter the first and second output Set Points (dialog screen 1)
   –Output Set Points, value 1 = 11, value 2 = 5 .

☐ Output assignments, (dialog screen 2):
   ☐ Enter OUT1 for Set Point 1, no inversion.
   ☐ Enter OUT2 for Set Point 2, no inversion.
   ☐ Enter OUT3 for Final Set Point, no inversion.
   ☐ Enter OUT4 for Timed Final Set Point, no inversion.
   ☐ Enter Pulse Width for Timed Final Set Point (x0,02 sec) = 20.

☞ **Note:**   Check the other counters with their default output assignement,
because multiple usage is prohibited.

3.3.5.2   Configuration of Final Set Point Value and counter characteristics
(see above)
From the Data Reference Screen for this counter select the 4x – register,
(defined in Figure 22 on page 51) and specify Set Point Value.

☐ Specify Set Point Value:
   ☐ Enter the Final Set Point Value (E/S) as 32–bit value (with user program):
      –E/S3: 400107 = 30 LD (see also page 31)

☐ Specify counter characteristics as:
   ☐ Enter parallel differential counter (0011), counting down (1000):
      –400101 – register = 3800 **hex**,
      relative Set Point (0001), (with user program):
      –400100 – register = 00**1**0 **hex** (see also page 31).

Caution: For counter 4, only the selections "Input Signal counts on:" and "Use Input 4 for Counter Enable" are useable. All other assignements were ignored. The references of 3x– and 4x–register for counter 4 can not be used.

3.3.6 Start Differential Counter

Start the controller, then from module data reference screen:

Step 1 Load/start counter:
–Enter LS3 bit in 400101– register (D8 = "1" resp. 3900 **hex)**
(with user program), (see also page 31) (Output structure).

Effect This enables the differential counter.

Effect The outputs switch to "1" signal and the counter's actual value is set to 0:
–300101 – register:
   VA1E3(D2) = OUT1 = "1" signal
   VA2E3(D10) = OUT2 = "1" signal
–300100 – register:
   E/SE3 (D10) = OUT3 = "1" signal.
–300106 –register:
   counter's actual value = 30

Note: The register bits VA1E4 = VA2E4 = E/SE4
from counter 4 are always = 0

Effect The pulses for counter 3 count up and the pulses for counter 4 count down (Counter / Clock input 3 / 4):
–at actual difference value11 OUT1 switches off,
–at actual difference value 5 OUT2 switches off,
–at actual difference value 0 OUT3 switches off and
–the Timed Final Set Point (Dynamic Final Signal) output OUT4 switches on for 400 ms.

If the counter has not reached the Final Set Point Value (Final Signal Value), the outputs OUT1 .. OUT4 can be switched off with a "1" signal in the 400101 – register BEA3 bit (with D10 = "1" resp. 3C00 hex, since the operating mode must be retained). That means all outputs and the input status word bits (300100 – register (D10), 300101–register (D2 and D10)) switche to "0" signal. See also page 13, Figure 5Relationship diagram.

A restart is possible through a rising edge at the 400101 – register ST3 bit (D9, resp. 3A00 hex), provided that the Final Set Point Value (actual value 0 in our

example) has not been reached.
You can Restart only after output switch–off (BEA). Refer to page
12Relationship diagram..
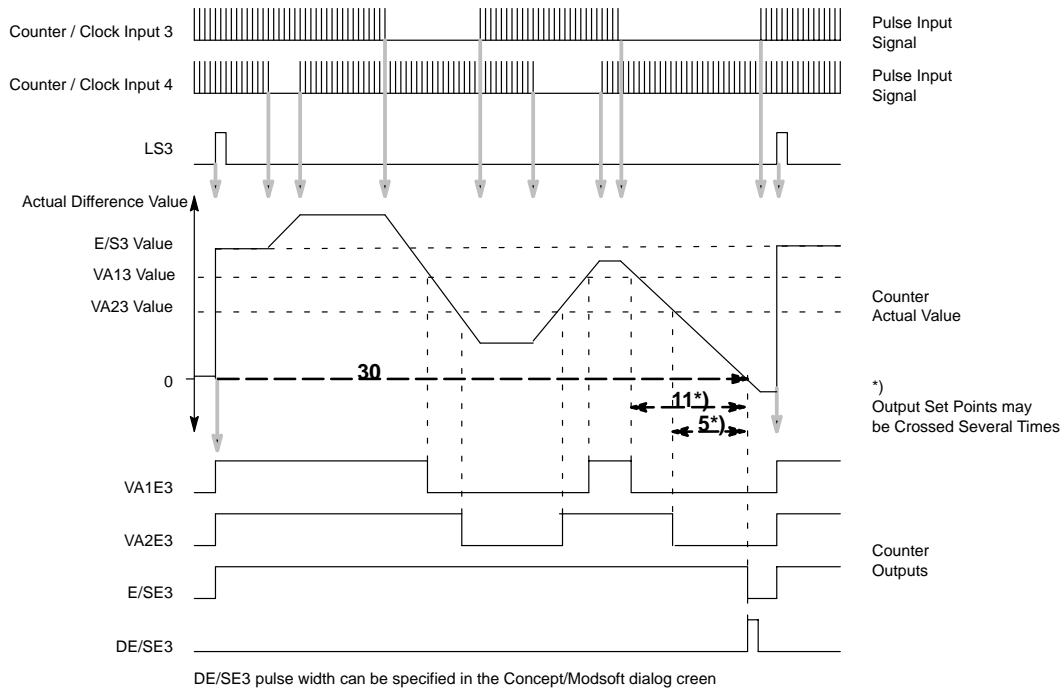
3.3.7   Example 3 Timing Diagram

Figure 32   Differential counter with parallel set–point cutoffs (VR = "1")

☞ **Note:**   If pulses continue to appear at counter inputs 3 / 4 after reaching the
Final Set Point Value (0), the pulses will also be counted and displayed as the
current actual value in the 300106– register as a 32–bit value.

When the counter is reset (Load/Start) the counting value is set to 30 and the
outputs became active again.

☞ **Note:**   If the counter's operating mode, counting direction, switch–off behavior,
or type of Set Point are changed while the counter's output signals are active,
the output will be deactivated and the new changes will take effect.

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3.4 Example 4: Event Counter (Up, Absolute) with Timed Set Point output activation, mode A

3.4.1 Specifications

This application describes using the counter 4 as an event counter with Timed Set Point output activation, counting up to 30 counts. See the following specification for conter 4.

Setpoint	Linked Outputs	Active Level	Values
FSP	07	0 –> 1 (2 sec)	30 counts
1SP	05	0 –> 1 (2 sec)	5 counts
2SP	06	0 –> 1 (2 sec)	11 counts
TFSP	08	0 –> 1 (2 sec)	

☞ **Note:** The values for the Set Points are in relative mode.

☐ Input Pulse is 24V, not inverted.

☐ A Field Signal is connected to input 8 and forces output switch–off.

☐ Input 4 is selected to enable the counter.

☐ The OR logic for the inputs sets the counter.

☐ Watchdog timer is shut off.

☐ IN7 is used to Load / Start, Restart counter.

☐ If communication is lost, the counter outputs will be set to 0.

3.4.2 Hardware Setup

Install the EHC 105 module into the local backplane's slot 8 and secure it. Install the module terminal strip and connect an external 24 VDC supply voltage (+ pin 40/– pin 39).

Connect the Pulse input signal to pin 17 (24VDC)

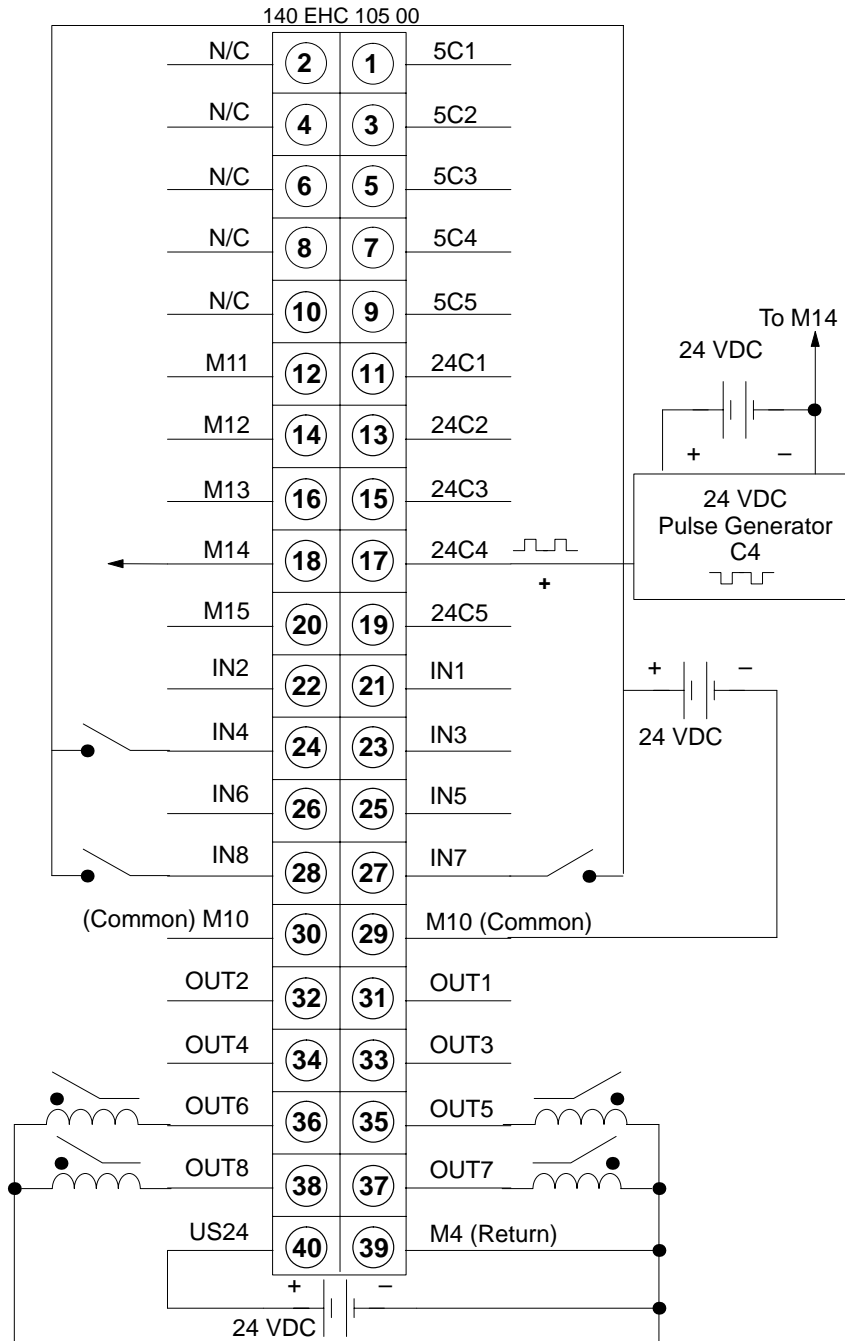☐ Module wiring can be found on the next page:

Figure 33   Wiring for example 1, event counter

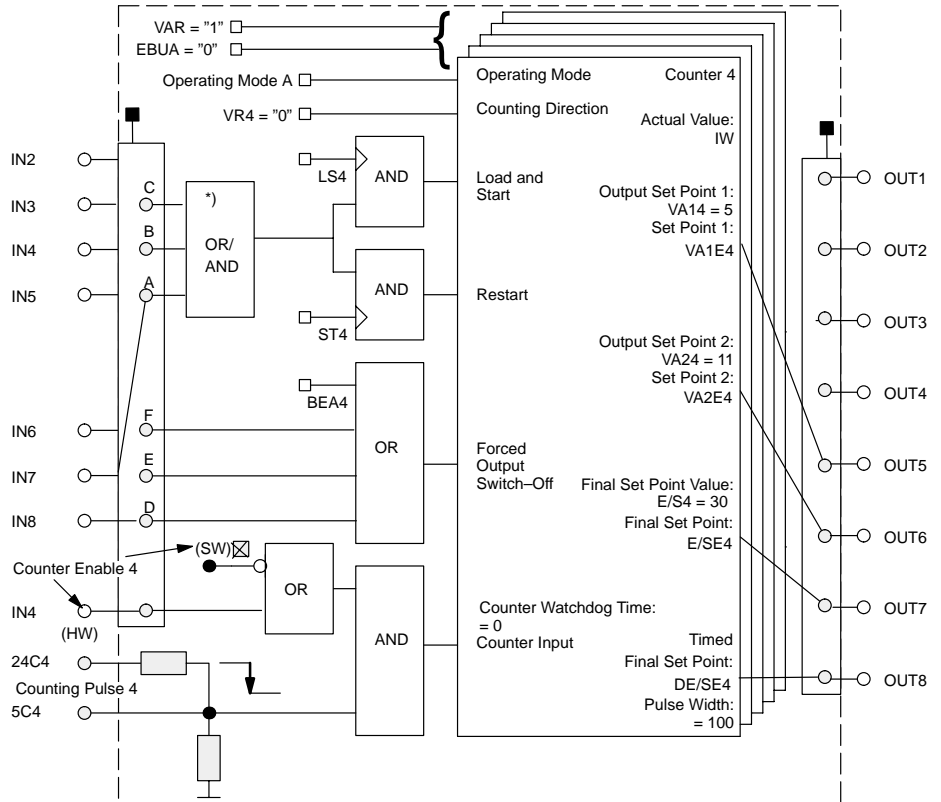### 3.4.3　Schematic for Example 4, Event Counter 4

Figure 34　Circuit diagram

⚠ **Caution:　Do not use outputs OUT1...OUT4 with other counters, as such multiple useage is prohibited.**

3.4.4   Software Settings using Concept

I / O Map screen (refer to example 1, page 49)

Example 4 I/O Configuration

```
┌─────────────────────────────────────────────────────────────────────────┐
│ ■                          140 EHC 105 00                                 │
├─────────────────────────────────────────────────────────────────────────┤
│ ┌─Inversion of Inputs───────────────────────────────────────────────────┐ │
│ │  ☐ No. 1   ☐ No. 2   ☐ No. 3   ☐ No. 4   ☐ No. 5   ☐ No. 6   ☐ No. 7   ☐ No. 8 │ │
│ └───────────────────────────────────────────────────────────────────────┘ │
│ ┌─Counter───────────────────────────────────┐ ┌─Outputs─────────────────┐ │
│ │          Counter: │4│ ⭥                    │ │ ┌─Preceded Signal 1─────┐ │ │
│ │                                            │ │ │ Output No: │5│ ⭥ ☐ Invert │ │
│ │  ┌──────────────────────────────────────┐  │ │ └───────────────────────┘ │ │
│ │  │ ☐ Invert Counter ☒ Input No. 4 for   │  │ │ ┌─Preceded Signal 2─────┐ │ │
│ │  │              Counter Enable          │  │ │ │ Output No: │6│ ⭥ ☐ Invert │ │
│ │  │ Counter Watchdog Time (x 0.1s): │0│  │  │ │ └───────────────────────┘ │ │
│ │  └──────────────────────────────────────┘  │ │ ┌─Final Signal──────────┐ │ │
│ │  ┌─Preceded Setpoint─────────────────────┐ │ │ │ Output No: │7│ ⭥ ☐ Invert │ │
│ │  │ Value 1: │5│      Value 2: │11│       │ │ │ └───────────────────────┘ │ │
│ │  └───────────────────────────────────────┘ │ │ ┌─Dynamic Final Signal──┐ │ │
│ │  ┌─Inputs─────────────────────────────────┐│ │ │ Output No: │8│ ⭥ ☐ Invert │ │
│ │  │┌─Load/Start or Restart────────────────┐││ │ └───────────────────────┘ │ │
│ │  ││ Logic Between Start Inputs │OR│ ⭥     │││ │                           │ │
│ │  ││ Input No: │7│⭥ Input No: │–│⭥ Input No:│–│⭥│││ Pulse Width (x 0.02 s): │100│ │
│ │  │└──────────────────────────────────────┘││ │                           │ │
│ │  │┌─Outputs Switch–Off───────────────────┐││ └───────────────────────────┘ │
│ │  ││ Input No: │8│⭥ Input No: │–│⭥ Input No:│–│⭥││                             │
│ │  │└──────────────────────────────────────┘││                               │
│ │  └────────────────────────────────────────┘│                               │
│ └────────────────────────────────────────────┘                               │
│  ┌──────────┐         ┌──────────┐              ┌──────────┐                  │
│  │    OK    │         │  Cancel  │              │   Help   │                  │
│  └──────────┘         └──────────┘              └──────────┘                  │
└─────────────────────────────────────────────────────────────────────────┘
```

3.4.4.1   I / O Configuration (see above)

You must stop the controller before configuring the module.

These are the selections to configure the counter.

☐ Counting pulse 1 with falling edge: no inversion, active–high.
  ☐ Counter Watchdog Time (x0,1s) = 0.

☐ Counter enable assignment to IN4:
  ☐ Input 4 for counter enable is selected.

☐ Load/start or restart and output switch–off assignments:
  ☐ Logic Between Start Inputs: OR.
  ☐ Enter IN7 as load/start or restart input, no inversion (no cross).
  ☐ Enter IN8 as output switch–off, no inversion (no cross).

☐ Output assignments, features (dialog screen):
  ☐ Enter OUT5 for Preceded Signal 1, no inversion (no cross).
  ☐ Enter OUT6 for Preceded Signal 2, no inversion (no cross).
  ☐ Enter OUT7 for Final Signal, no inversion (no cross).
  ☐ Enter OUT8 for Dynamic Final Signal, no inversion (no cross).

□ Dynamic Final Signal Pulse Width (x0,02 s) = 100.

☞ **Note:** Check the other counters with their default output assignement, because multiple usage is prohibited.

□ Enter the first and second Preceded Setpoint:
  –Preceded Set Points, value 1 = 5, value 2 = 11 .

3.4.4.2 Configuration of Final Signal Value and counter characteristics
(see above)
From the Data Reference Screen for this counter select the 4x – register, (defined on page 49)(I/O Map screen) and specify Set Point Value.

□ Specify Final Signal Value:
  □ Enter the Final Signal Value (E/S) as 32–bit value (with user program):
    –E/S4: 400109 = 30 LD (see also page 31) (Output structure).
□ Specify counter characteristics:
  □ Enter parallel timed event counter (1010), counting up (0000):
    –400102 – register = 00**A**0 **hex** (see also page 31) (Output structure).,
    absolute Set Point (0000), (with user program):
    –400100 – register = 00**0**0 **hex.**

3.4.5 Software Settings using Modsoft

I / O Map screen (refer to example 1)

Example 4 I/O Configuration

For Inputs

```
  Hex       Dec      Bin       GoTo                                    Quit
  F1 —— F2 —— F3 —— F4   I / O Map Module Editor · F7−Lev 8−F8−OFF —— F9 ——
                   140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 7 of 10
                                    COUNTER 4
   Head Slot: 0 Drop: 1      Slot: 8
   INPUTS:. . .                       (next screen for counter 1 output settings)
   Input Signal counts on: Neg Transition    Use Input 4 for Counter enable: Yes

   Counter 1 Watchdog Time = 0          DEC        (*0.1sec.)

   Output Setpoint 1, Value 1= 5        DEC
   Output Setpoint 2, Value 2= 11       DEC
                          Counter Starts or Restarts . . .
       Input A: 7           Input B:NONE             Input C: NONE
   Logic function for inputs to START / RESTART Counter: OR

   Freeze Counter's register for PLC update and Switch Outputs off with....
       Input D:. 8        or Input E:.NONE        or Input F: NONE
   - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   Invert Control Inputs . . .                 (applies to all five count-
   ers)
   No. 1: NO               No. 2: NO                No. 3: NO
   No. 4: NO               No. 5: NO                No. 6: NO
   No. 7: NO         Page up / down for prev / next screen
```

For Outputs

```
  Hex       Dec      Bin       GoTo                                    Quit
  F1 —— F2 —— F3 —— F4   I / O Map Module Editor · F7−Lev 8−F8−OFF —— F9 ——
                   140 EHC 105 00: HIGH SPEED COUNTER, 5 Chan  Screen 8 of 10
                              COUNTER 4 (cont.)
   Head Slot: 0 Drop: 1       Slot: 8
   OUTPUTS:  . . .             (Prev Screen for this counter's 4 input settings)
   WARNING: DO NOT SELECT THE SAME OUTPUT WITH MORE THAN ONE SET POINT!

   Set Point 1 Linked to Output=           5          Invert: NO

   Set Point 2 Linked to Output=           6          Invert: NO

   Final Set Point Linked to Output=       7          Invert: NO

   Timed Final Set Point Linked to Output=  8         Invert: NO

   Pulse Width for Timed Final Set Point=  100   DEC  (*0.02):
   - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - - -
   Invert Control Inputs . . .              (applies to all five counters)
   No. 1: NO               No. 2: NO                No. 3: NO
   No. 4: NO               No. 5: NO                No. 6: NO
   No. 7: NO               No. 8: NO
                   Page up / down for prev / next screen
```

Figure 35   Modsoft dialog screen

3.4.5.1   I / O Configuration (see above)
You must stop the controller before configuring the module.

Use the following selections to configure the counter.

☐ Input Signal counts on: neg. transition.
   ☐ Counter 4 Watchdog Time (x0,1sec) = 0

☐ Counter enable assignment to IN4, (dialog screen 7):
   ☐ Use Input4 for counter enable: Yes.

☐ Load/start or restart and output switch–off assignments,(dialog screen 7):
   ☐ Logic function for inputs to Start / Restart Counter: OR.
   ☐ Enter IN7 as Starts or Restarts Counter, no inversion.
   ☐ Enter IN8 as Freeze Counter's register for PLC update and Switch
     Outputs off (no inversion of IN8).

☐ Enter the first and second output Set Points (dialog screen 7)
   –Output Set Points, value 1 = 5, value 2 = 11 .

☐ Output assignments, (dialog screen 8):
   ☐ Enter OUT5 for Set Point 1, no inversion.
   ☐ Enter OUT6 for Set Point 2, no inversion.
   ☐ Enter OUT7 for Final Set Point, no inversion.
   ☐ Enter OUT8 for Timed Final Set Point, no inversion.
   ☐ Enter Pulse Width for Timed Final Set Point (x0,02 sec) = 100.

☞ **Note:**   Check the other counters with their default output assignement,
because multiple usage is prohibited.

3.4.5.2   Configuration of Final Set Point Value and counter characteristics
(see above)
From the Data Reference Screen for this counter select the 4x – register,
(defined in Figure 22 on page 51) and specify Set Point Value.

☐ Specify Set Point Value:
   ☐ Enter the Final Set Point Value (E/S) as 32–bit value (with user program):
   –E/S4: 400109 = 30 LD (see also page 31)

☐ Specify counter characteristics as:
   ☐ Enter timed event counter (1010), counting up (0000):
   –400102 – register = 00**A**0 **hex** (see also page 31),
   absolute Set Point (0000), (with user program):
   –400100 – register = 00**0**0 **hex.**

3.4.6   Start Counter 4

Start the controller, then from module data reference screen:

Step 1   Load/start counter:
–Activate (High) discrete input 7 (pin 27) .
–Enter LS4 bit in 400102 – register (D0 = "1" resp. 00**A1 hex)** (with user program), (see also page 31) (Output structure).

Effect   The register for outputs switch to "1" signal and the counter's actual value is set to 0:
–300101 – register:
   VA1E4(D3) = "1" signal
   VA2E4(D11) = "1" signal
–300100 – register:
   E/SE4(D11) = "1" signal;
–All outputs switches off (Out 5, 6, 7, 8).
–Counter's actual value = 0.

Step 2   Enter "1" signal on discrete input IN4 (pin 24, counter enable). This enables the counter 4.

Effect   Counter 4 counts the pulses at counter input 4:
–at actual value 5, OUT5 switches on for 2 sec,
–at actual value 11, OUT6 switches on for 2 sec,
–at actual value 30, OUT7 switches on for2 sec and
–the timed output OUT8 also switches on for 2 sec.

☞   **Note:**   The register signals from counter 4 have following states:
–at actual value 5 = VA1E4 switches off,
–at actual value 11 = VA2E4 switches off,
–at actual value 30 = E/SE4 switches off.

If the counter has not reached the Final Set Point Value (Final Signal Value), the outputs OUT5 .. OUT8 can be switched off with an external "1" signal connected to input IN8 or through the 400102 – register BEA4 bit (with D2 = "1" resp. 00A4 hex, since the operating mode must be retained). That means all outputs and the input status word bits (300100 – register (D11), 300101–register (D3 and D11)) switche to "0" signal. See also page 20, Figure 10Operating mode A.

A restart is possible through discrete input IN7 and a rising edge at the 400102 – register ST4 bit (D1, resp. 00A1 hex), provided that the Final Set Point Value (actual value 30 in our example) has not been reached. You can Restart only after output switch–off (BEA). Refer to page 12Relationship diagram.
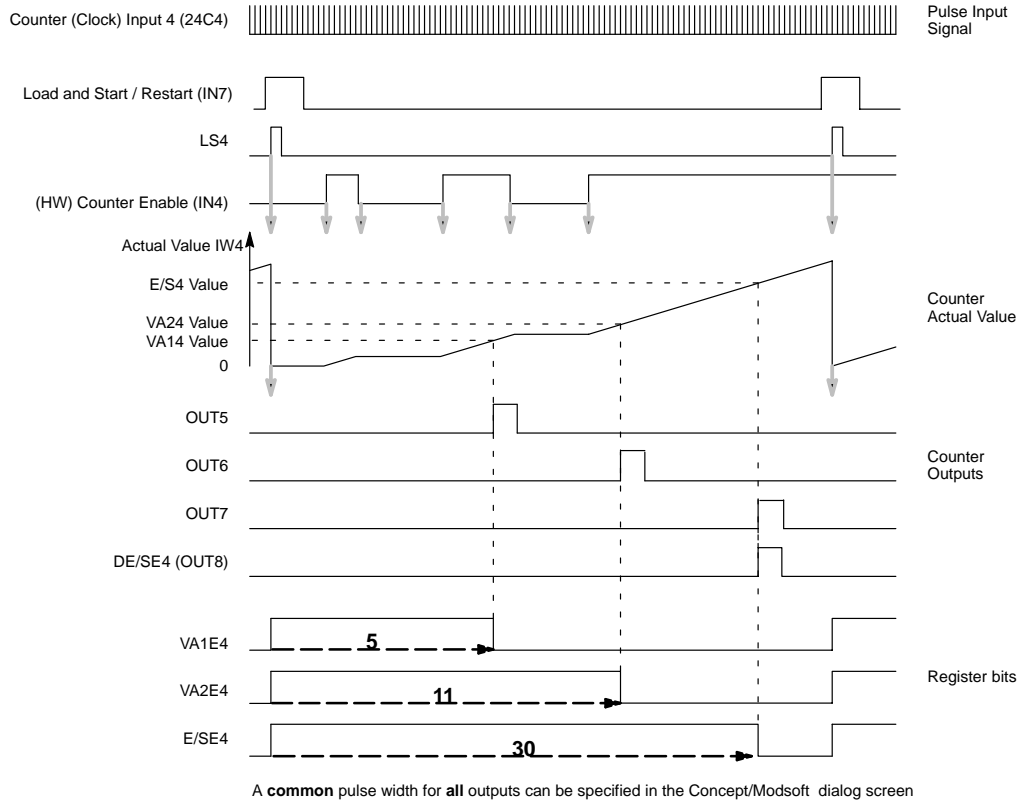
3.4.7 Example 4 Timing Diagram

| Counter (Clock) Input 4 (24C4) | | Pulse Input Signal |

Load and Start / Restart (IN7)

LS4

(HW) Counter Enable (IN4)

Actual Value IW4

E/S4 Value

VA24 Value
VA14 Value

0

Counter Actual Value

OUT5

OUT6 — Counter Outputs

OUT7

DE/SE4 (OUT8)

VA1E4 — **5**

VA2E4 — **11** — Register bits

E/SE4 — **30**

A **common** pulse width for **all** outputs can be specified in the Concept/Modsoft dialog screen

Figure 36 Counting up (VR = 0)

☞ **Note:** If pulses continue to appear at counter input 4 after reaching the Final Set Point Value (30), the pulses will also be counted and displayed as the current actual value in the 300108– register as a 32–bit value.

When the counter is reset (Load/Start) the counting value is set to 0, the outputs became inactive and the register bits will be active again.

☞ **Note:** If the counter's operating mode, counting direction, switch–off behavior, or type of Set Point are changed while the counter's output signals are active, the output will be deactivated and the new changes will take effect.

Chapter 4
Concept EHC 105 Derived Data Types

Derived data types simplify access to the EHC 105's input and output signals.

The EHC 105 is mapped to word registers. The derived data type structures provided are composed of bytes and double words (WORD 32). Should you wish to have access to individual bits, the corresponding bytes must first be converted to bit strings.

The following derived data types are available for the EHC 105:

Table 11   EHC 105 derived data types

Derived Data Types	Valid for	Memory Utilization
EHC105_IN	EHC 105 input data	12 input words
EHC105_OUT	EHC 105 output data	13 output words

Table 12   EHC105_IN: EHC 105 input data

Element	Data Type	Function
error	BYTE	Error flag status byte Bit 0 = 1: Counter 1 error (ERR1) Bit 1 = 1: Counter 2 error (ERR2) Bit 2 = 1: Counter 3 error (ERR3) Bit 3 = 1: Counter 4 error (ERR4) Bit 4 = 1: Counter 5 error (ERR5) Bit 5 = 1: Clock error, Bit 5 = 0: Counter overflow Bit 6 = 1: Output short circuit Bit 7 = 1: External power failure
Final	BYTE	Switch–off signals status byte Bit 0 = 1: Counter 1 Final Set Point (E/SE1) Bit 1 = 1: Counter 2 Final Set Point (E/SE2) Bit 2 = 1: Counter 3 Final Set Point (E/SE3) Bit 3 = 1: Counter 4 Final Set Point (E/SE4) Bit 4 = 1: Counter 5 Final Set Point (E/SE5)
Set Point 1	BYTE	Switch–off signals status byte Bit 0 = 1: Counter 1 1st Set Point (VA1E1) Bit 1 = 1: Counter 2 1st Set Point (VA1E2) Bit 2 = 1: Counter 3 1st Set Point (VA1E3) Bit 3 = 1: Counter 4 1st Set Point (VA1E4) Bit 4 = 1: Counter 5 1st Set Point (VA1E5)
Set Point 2	BYTE	Switch–off signals status byte Bit 0 = 1: Counter 1 2nd Set Point (VA2E1) Bit 1 = 1: Counter 2 2nd Set Point (VA2E2) Bit 2 = 1: Counter 3 2nd Set Point (VA2E3) Bit 3 = 1: Counter 4 2nd Set Point (VA2E4) Bit 4 = 1: Counter 5 2nd Set Point (VA2E5)
actual	ARRAY[1..5] OF WORD32	Actual Values 1st WORD 32: Counter 1 Actual Value 1 2nd WORD 32: Counter 2 Actual Value 2 3rd WORD 32: Counter 3 Actual Value 3 4th WORD 32: Counter 4 Actual Value 4 5th WORD 32: Counter 5 Actual Value 5

Note: Further information see chapter 1.4.1, starting page 28Input Structure.

Table 13   EHC105_OUT: EHC 105 Output Data

Element	Data Type	Function
quit	BYTE	Bit 0 = 1: Output short circuit acknowledgement (Q) Bit 1 = 1: Acknowledgement for under voltage and counter errors (FQ). Bit 2 = Don't care. Bit 3 = Don't care. Bit 4 = 1: Set–point cutoff in "relative" mode, otherwise "absolute" (VAR). Bit 5 = 1: All output states retained on failure (EBUA). Bit 6 = Don't care. Bit 7 = Don't care.
control	ARRAY[1..5] OF BYTE	BYTE 1 to 5: Control bytes Counters 1 through 5 Bit 0 = 1: Load/start (LSx) Bit 1 = 1: Restart (STx) Bit 2 = 1: Output switch–off (BEAx) Bit 3 = 0: Up–counter, Bit 3 = 1: Down–counter (VRx) Bits 4..7: Counter operation mode (see Table 1 , page 16)
Final	ARRAY[1..5] OF WORD32	Final Set Point Values 1st WORD 32: Counter 1 Final Set Point Value (E/S1) 2nd WORD 32: Counter 2 Final Set Point Value (E/S2) 3rd WORD 32: Counter 3 Final Set Point Value (E/S3) 4th WORD 32: Counter 4 Final Set Point Value (E/S4) 5th WORD 32: Counter 5 Final Set Point Value (E/S5)

☞ **Note:**   Further information see chapter 1.4.2 , starting page 30 Output Structure.

Concept EHC 105 Derived Data Types   85

Appendix A
Module Description

140 EHC 105 00
High–Speed Counter
Module Description

The following hardware–specific details are presented here for the EHC 105 counter module:

☐ Module View

☐ Features

☐ Operations

☐ Configuration

☐ Technical Specifications
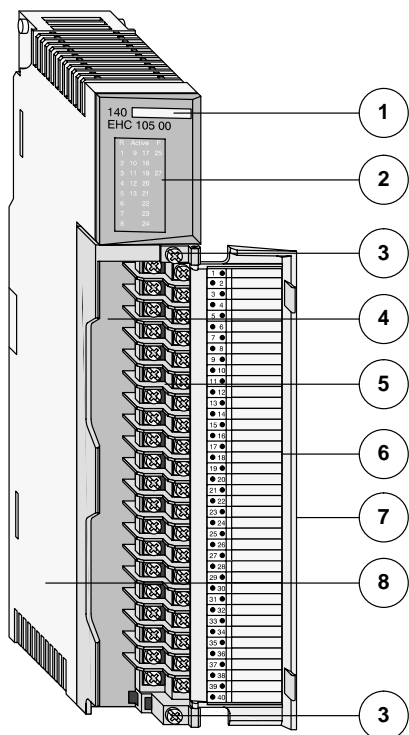
Figure 37
EHC 105 module front view

Positions of the User–Accessable Parts

1 Color Code
2 LED Status Display
3 I/O Block Mounting Screws
4 I/O Block
5 Terminal Block
6 Label Inlay (Inner Side)
7 I/O Block Cover
8 Standard–Size Module (Housing)

1   Features

The EHC 105 module is a high–speed counter with the following features:

☐ Counted value processing for 5 pulse generators (counter inputs isolated
  from one another)
  (5 VDC, f_{max} = 100 kHz for cable lengths of up to 100 m)
  (24 VDC, f_{max} = 20 kHz for cable lengths of up to 100 m)

☐ 8 isolated inputs and outputs with LED status display

☐ Short circuit–proof output

☐ Backplane provides the internal 5 VDC supply

☐ Configuration assignment is made by the CPU

1.1   Hardware

1.1.1   Voltage Supply
The EHC 105 module is supplied by the Quantum–Bus with VCC = 5 VDC. The
isolated I/O and the counter inputs are an exception. They receive the working
voltage US24 = 24 VDC provided by an external power supply. The green (P)
LED lights when US24 is present.

In addition, if the 24 VDC is not present, status bit 7 is set and the F–LED turns
on. If the 24 VDC is present again, status bit 7 is reset and the F–LED turns off.

☞ **Note:**   The alternatively available 5 VDC counter inputs may also be used.

1.1.2   Hot Swap
As for all Quantum module, you can remove and insert the module during bus
operation. However, module reconfiguration is required.

1.1.3   Discrete Inputs

The module is equipped with 5 counter and 8 discrete inputs, each of which can be assigned different functions.

Counter Inputs: The counter inputs are isolated from one another and from the discrete I/O. Each counter input is present in two variations, whereby 5C1...5C5 are for 5 VDC signals and 24C1...24C5 for 24 VDC signals.

STOP

Warning: Only transmitters with 5 VDC output signals may be connected to 5C1...5C5. From each counter input only one connection (either 5 VDC or 24 VDC) may be utilized.

There is exactly one reference potential per counter input (M11...M15) i.e.:
5 VDC transmitter on counter 4: using terminals 5C4 and M14
24 VDC transmitter on counter 4: using terminals 24C4 and M14

Every counter is assigned a hardware–related input (IN1...IN5) as counter enable (gate function). Whether the input is to be used as counter enable can be selected separately for each counter channel through the configuration dialogs of Concept or Modsoft. The input may be used for other functions, should it not be allocated as counter enable. The counter input is then always enabled.

All input signals are displayed by green LEDs. (Refer to LED Status Display)

Discrete Inputs Discrete inputs are isolated from the back plane, counter inputs and the outputs.

The discrete inputs can be assigned the following functions:

☐ Counter enable (gate function)

☐ Counter load/start (outputs set)

☐ Counter restart (outputs set)

☐ Output switch–off trigger (resets outputs VA1Ex, VA2Ex and E/SEx)

☐ Input signal states can be inverted

The "load/start" resp. "restart" functions are "AND"ed with the LSx resp. STx state RAM bits.

Note: If no hardware input is utilized for "load/store" resp. "restart", then the "AND" condition is met if the bit in state RAM is set.

In the event counter (modes 1 and 2) and differential counter (modes 3 and 4) operating modes, the "restart" command is only possible after an "output switch–off" (BEAx).

The "restart" command is not possible in the repetitive counter (mode 5), velocity counter (modes 6 and 7), and event counter with fast output switch–off (modes 8 and 9) operating modes.

The functions can be chosen in the Concept I/O mapping list with the "Params" button or through the Modsoft configuration screens.

Every input is assigned a green LED in the LED status display.

1.1.4 Discrete Outputs

The module has 8 discrete outputs. All outputs are short circuit and overload–proof (I_{max} = 500 mA), and have potential isolation in respect to the inputs and back plane (I/O bus).

The outputs can be assigned the following functions:

☐ First Set Point (timed for mode A)

☐ Second Set Point (timed for mode A)

☐ Final Set Point (timed for mode A)

☐ Timed Final Set Point (with choice of pulse width)

☐ Output signal states can be inverted

The functions can be chosen in the Concept I/O map with the "Params" button or through the Modsoft configuration screens.

Display: green LEDs (refer to LED Status Display)

Short circuit of one or more outputs leads to a fault message (the red LED (F) lights). As soon as the short circuit has been neutralized, the outputs can be returned to normal operation per collective reset signal "Q".

☞ **Note:** At power–up (back plane 5 VDC) all discrete outputs are inactive. On master station failure all outputs are deactivated. (The outputs go to "0" with positive logic and "1" with negative logic).

1.1.5 Counter

5 equivalent, independently usable counters with the following functions are utilized:

☐ 32–bit event counter with 6 modes

☐ 32–bit differential counter (2 configurable counter pairs) with 2 modes

☐ 16–bit repetitive counter

☐ 32–bit (velocity counter) with 2 modes

1.1.6 Jumpers

The module is delivered without jumpers. The module's contact strips are only used for test purposes.

1.1.7 LED Status Display
LED Status Display Front View (LED Numbering)

```
┌─────────────────────────────────┐
│  R        ACTIVE        F        │
│  ▶1      ▶C1      1▶     P        │
│  ▶2      ▶C2      2▶              │
│  ▶3      ▶C3      3▶              │
│  ▶4      ▶C4      4▶              │
│  ▶5      ▶C5      5▶              │
│  ▶6              6▶              │
│  ▶7              7▶              │
│  ▶8              8▶              │
└─────────────────────────────────┘
```

Status displays:

☐ R(eady) LED (green):
  –lights when the module is ready (firmware initialization has been completed)

☐ P(ower) LED (green):
  –lights when the US24 working voltage is present

☐ ACTIVE LED (green):
  –lights as soon as the PLC communication becomes active

☐ LEDs ▶1 to ▶8 (green):
  –display the signal states of the discrete inputs IN1...IN 8

☐ LEDs 1▶ to 8▶ (green):
  –display the signal states of the discrete outputs OUT1...OUT8

☐ LEDs ▶C1 to ▶C5 (green):
  –light with the clock frequency applied to clock–inputs 5C1 resp. 24C1 to 5C5 resp. 24C5

Fault display:

☐ F(ault) LED (red) lights on the following faults:
  – 24 VDC supply voltage (US24) is not present
  –short circuit on one of the OUTn outputs
  –pulse monitoring has tripped (Indicate bit = "1" and ERRx = "1")
  –counter overflow (Indicate bit = "0" and ERRx = "1")

2 Operation

The module can operate in the following modes:

☐ Event counter with parallel Set Point output activation
☐ Event counter with parallel Set Point output activation and fast Final
   Set Point
☐ Event counter with serial Set Point activation
☐ Event counter with serial Set Point activation and fast Final Set Point
☐ Event counter with timed Set Point output activation
☐ Event counter with latched Set Point output avtivation
☐ Differential counter with parallel Set Point output activation
☐ Differential counter with serial Set Point output activation
☐ Repetitive counter
☐ Rate counter with 100ms gate time
☐ Rate counter with 1s gate time

☞ **Note:**   For the operating mode assignments to their mode identifiers, refer
to Table 1 resp. page 16.

Module outputs assigned to the final set–point of those operating modes making
use of the fast final set–point are processed particularly fast:

☐ without fast Final Set Point: typically 3 ms
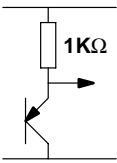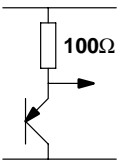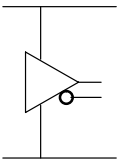☐ with fast Final Set Point: typically 0.5 ms

3 Configuration
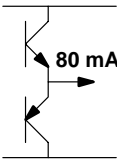
3.1 Cabling

☐ Shielded, twisted pair cable is to be utilized for pulse generator connection to the counter inputs.
  ▫ JE–LiYCY 2 X 2 X 0.5 (Order no.: 424 234 035)
  ▫ JE–LiYCY 5 X 2 X 0.5 (Order no.: 424 238 059)
☐ The shield should have a short connection (< 20 cm) with ground at one cable end.
☐ Be sure not to install the cabling together with power lines or other similar sources of electrical disturbance. Clearance > 0.5 m.
☐ Input connecting cables, bulk

  ▫ JE–LiYCY 2 X 2 X 0.5 twisted pair, (Order no.: 424 234 035).
  ▫ JE–LiYCY 5 X 2 X 0.5 twisted pair, (Order no.: 424 238 059).

Note: Pay attention to cable length dependencies upon transmitter frequencies and output type .

Table 14   Max. cut–off frequencies in respect to transmitter output type and cable length

Transmitter Output	Circuit Diagram	Transmitter Output Level (VDC)	Cable Length (m)	Max. Transmitter Frequency kHz
Push–pull driver	80 mA	24 24 24	30 100 300	35 20 10
NPN driver (open collector)	1KΩ	24 24 24	30 100 300	35 20 10
NPN driver (open collector)	100Ω	5 5	30 300	100 100
SN 75 176 line driver		5 5	30 300	100 100

3.2 Connection and Signal Allocation (I/O Block)

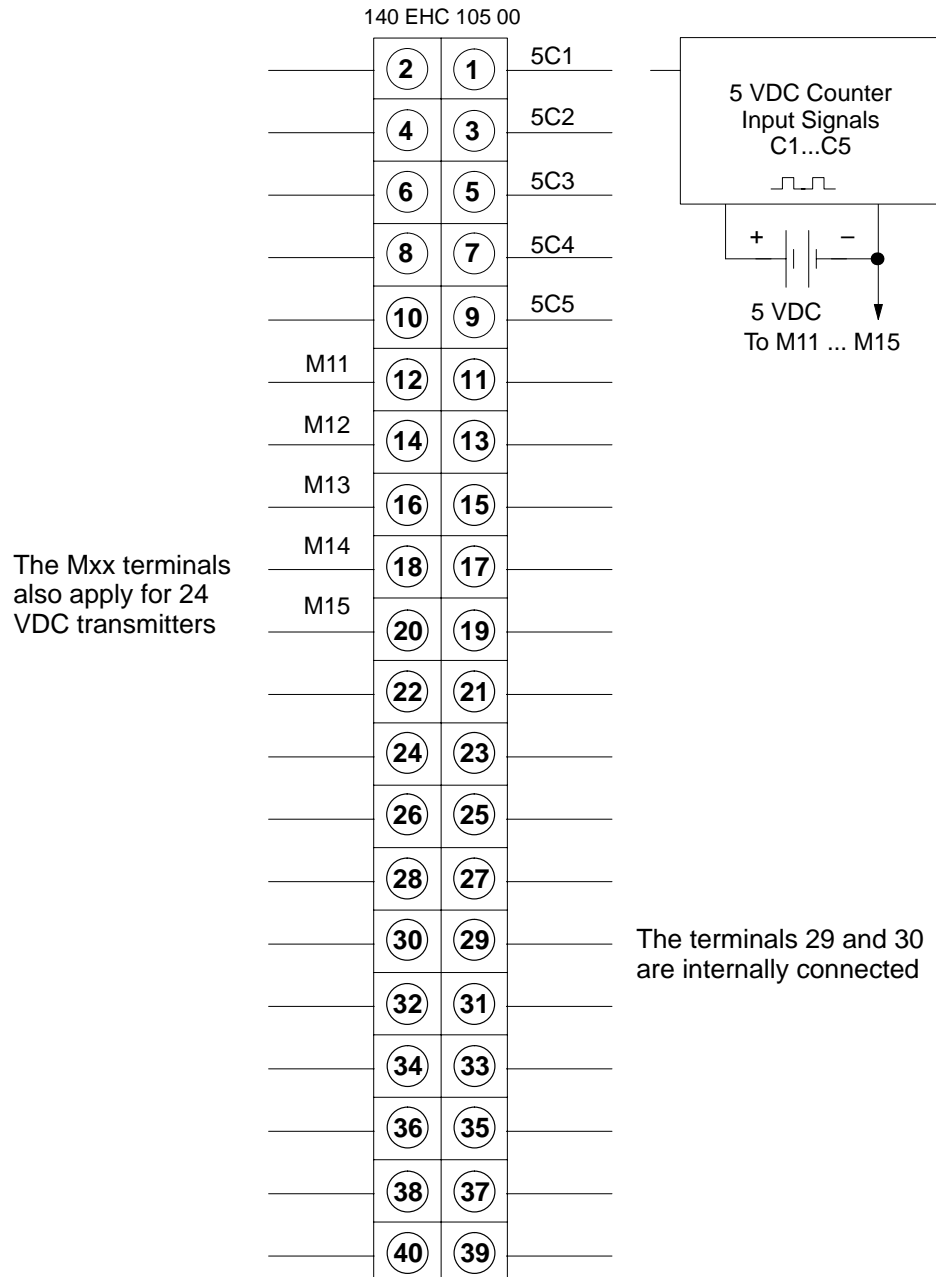### 3.2.1 Wiring diagram for 5Cx counter inputs

Figure 38   5 VDC counter inputs
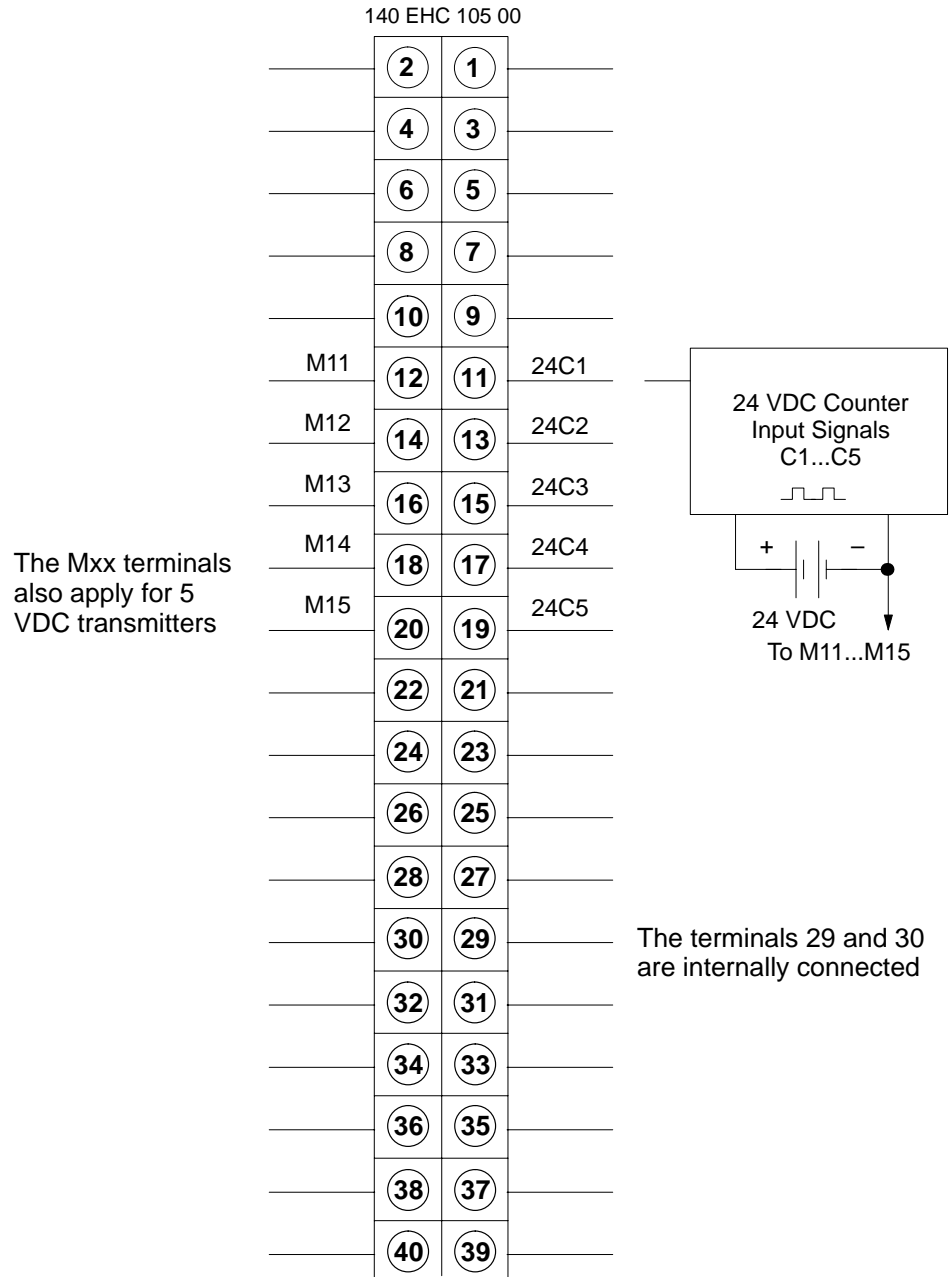
3.2.2 Wiring diagram for 24Cx counter inputs

140 EHC 105 00

	2	1
	4	3
	6	5
	8	7
	10	9
M11	12	11	24C1
M12	14	13	24C2
M13	16	15	24C3
M14	18	17	24C4
M15	20	19	24C5
	22	21
	24	23
	26	25
	28	27
	30	29
	32	31
	34	33
	36	35
	38	37
	40	39

24 VDC Counter
Input Signals
C1...C5

+ −

24 VDC
To M11...M15

The Mxx terminals also apply for 5 VDC transmitters

The terminals 29 and 30 are internally connected

Figure 39   24V counter inputs

3.2.3 Wiring diagram for discrete inputs and outputs

140 EHC 105 00

Left			Right
N/C	2	1	5C1
N/C	4	3	5C2
N/C	6	5	5C3
N/C	8	7	5C4
N/C	10	9	5C5
M11	12	11	24C1
M12	14	13	24C2
M13	16	15	24C3
M14	18	17	24C4
M15	20	19	24C5
IN2	22	21	IN1
IN4	24	23	IN3
IN6	26	25	IN5
IN8	28	27	IN7
(Common) M10	30	29	M10 (Common)
OUT2	32	31	OUT1
OUT4	34	33	OUT3
OUT6	36	35	OUT5
OUT8	38	37	OUT7
US24	40	39	M4 (Return)

N/C: No Connection

The terminals 29 and 30 are internally connected

24 VDC

24 VDC

Figure 40   Discrete signals

4   Technical Specifications

Specifications

Number of channels	5 counter inputs, 8 discrete inputs and 8 digital outputs
LEDs	**Active** **F** **R (Green)** Module is ready **1 ... 8 (Green – lft column)** Discrete Inputs (IN1 ... IN8) **C1 ... C5 (Green – middle column)** Counter Inputs (C1 ... C5) **1 ... 8 (Green – right column)** Discrete Outputs (OUT1 ... OUT8) **P (Green)**
Required Addressing	12 Words In 13 Words Out

Counter Inputs

Count Frequency (100KHz)	@5 VDC, further information see cable length Table 14 page 98.
Count Frequency (20KHz)	@24 VDC, further information see cable length Table 14, page 98.
Count to Output Assertion Delay (Max)	3ms
Input current	7 mA for 24 VDC, 8 mA for 3,1VDC
Duty Cycle	1 : 1
Data Formats	16 Bit Counter: 65.535 Decimal 32 Bit Counter: 2.147.483.647 Decimal
Delay Time (typical)	t = 0,002 ms
Max. Continous Input Voltage	30 VDC for 24 VDC Counter Inputs

Discrete Inputs

VREF Supply +24VDC	Off State (VDC) ON State (VDC) –3,0 ... 5,0 15,0 ... 30,0
Delay Time (typical) IN1 ... IN6 IN7, IN8	ton = 2,2 ms, toff = 1ms ton = 0,006 ms, toff = 0,3 ms
Input current (typical)	5 mA

Discrete Outputs

Switch ON	20 ... 30 VDC
Switch OFF	0 VDC (ground reference)
Max Load Current (each output)	0,5 A
Output Off State Leackage	0,1 mA max @ 30 VDC
Output On State Voltage Drop	1,5 VDC @ 0,5 A

Miscellaneous

Isolation (Channel to Bus)	500 VAC rms for 1 minute
Fault Detection	Loss of output field power, output short circuit
Power Dissipation	$\leq$ 6W
Bus Currend Required	250 mA
External 24 VDC Power Supply	19,2 ... 30 VDC, 24 VDC nominal, 60 mA reqired plus the load current for each output.
External Fusing	User discretion
Compatibility	Programming Software: see page 38. Quantum Controllers: see page 38.

☞ **Note:** The 5Cx and 24Cx counter inputs may be used alternatively.

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